8GB DDR3 – SDRAM ECC XR-DIMM™

240 Pin ECC XR-DIMM™

SGV08G72B1BB2SA-xx(W)RT

8GByte in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  - DDR3 1333 MT/s CL9 — -CC
  - DDR3 1600 MT/s CL11 — -DC
- Module density
  8GB with 18 dies and 2 ranks
- Standard Grade (T_A) 0°C to 70°C; (T_C) 0°C to 85°C
  Grade W (T_A) -40°C to 85°C; (T_C) -40°C to 95°C

Environmental Requirements:

- Operating temperature (ambient)
  - Standard Grade 0°C to 70°C
  - Grade W -40°C to 85°C
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Features:

- eXtreme Rugged 240-pin 72-bit DDR3 Small Outline Double Data Rate synchronous DRAM Module
- 67.5 mm x 38 mm module that stacks 7.36mm above CPU board
- Samtec BSH-120-01-X-D-A connector
- Socket ANSI/VITA 47-2005 shock and vibration compliant
- Module organization: dual rank 1G x 72
- V_{DD} = 1.5V ±0.075V, V_{DDQ} 1.5V ±0.075V
- 1.5V I/O (SSTL_15 compatible)
- Fly-by-bus with termination for C/A & CLK bus
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Compatible to XR-DIMM™ 2.0 specification of SFF-SIG (see www.sff-sig.org)
- The pcb and all components are manufactured according to the RoHS compliance specification
  [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR3 - SDRAM component : Samsung K4B4G0846B**
- 512Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit prefetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.
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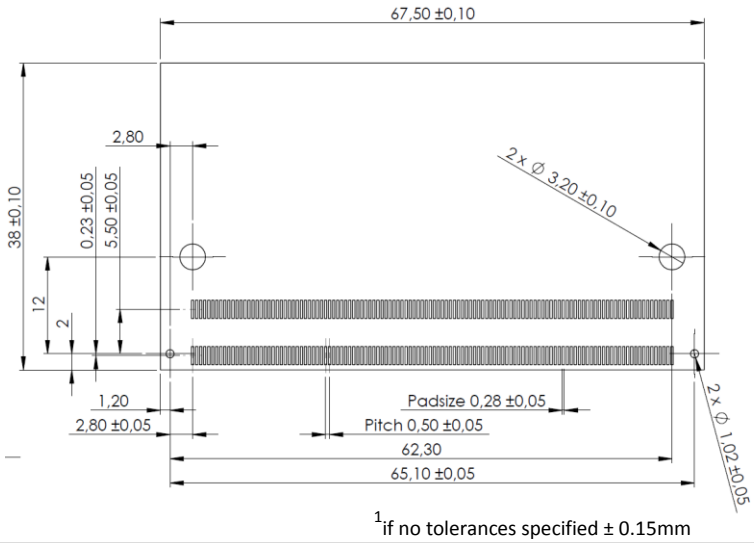
Figure: mechanical dimensions[1]



[1] if no tolerances specified ± 0.15mm

This Swissbit module is a highly ruggedized 240-pin 72bit DDR3 SDRAM ECC Small Outline module which is organized as 1Gx72 high speed CMOS memory arrays. Enhanced ruggedness is obtained through the use of a high-performance, 240-pin socket connector system and the use of standoffs with screw attachment firmly holding the CPU and memory module together. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.
The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the XR-DIMM manufacturer (Swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
1G x 72bit	18 x 512M x 8bit (4096Mbit)	16	BA0, BA1, BA2	10	8k	S0#,S1#

Module Dimensions in mm
67.5mm (long) x 38mm(high) x 7.36mm(standoff from CPU board)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SGV08G72B1BB2SA-CC[W]RT	8 GB	10.6 GB/s	1.50ns / 1333MT/s	9-9-9
SGV08G72B1BB2SA-DC[W]RT	8 GB	12.8 GB/s	1.25ns / 1600MT/s	11-11-11

Pin Name

Symbol	Type	Polarity	Function
A0–A15	IN	—	During a Bank Activate command cycle, address input defines the row address (RA0–RA14). During a Read or Write command cycle, address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC_n) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
BA0–BA2	IN	—	Selects which SDRAM bank of eight is activated.
CK0_t–CK1_t CK0_c–CK1_c	IN	Differential crossing	CK_t and CK_c are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK_t and negative edge of CK_c. Output (read) data is referenced to the crossing of CK_t and CK_c (Both directions of crossing).
CKE0- CKE1	IN	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
DM0–DM8	IN	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
DQ0–DQ63, CB0–CB7	I/0	—	Data and Check Bit Input/Output pins.
DQS0_t–DQS8_t DQS0_c–DQS8_c	I/O	Differential crossing	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0–DQ7 are associated with the LDQS_t and LDQS_c pins and Pins DQ8–DQ15 are associated with UDQS_t and UDQS_c pins.
ODT0-ODT1	IN	Active High	When high, termination resistance is enabled for all DQ, DQS_t, DQS_c and DM pins, assuming this function is enabled on the DRAM.
RAS_n, CAS_n, WE_n	IN	Active Low	RAS_n, CAS_n, and WE_n (along with S_n) define the command being entered.
RESET_n	IN	Active Low	The RESET_n pin is connected to the RESET_n pin on each DRAM. When low, all DRAMs are set to a known state.
S0_n S1_n	IN	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
VDD, VSS	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
VDDQ	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For the DDR3 XR-DIMM designs, VDDQ shares the same power plane as VDD pins.
VTT	Supply		Termination voltage for C/A & Control bus, by default at VDD/2
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.
VREFDQ	Supply		Reference voltage for I/O inputs, by default at VDD/2
VREFCA	Supply		Reference voltage for command/address/control inputs, by default at VDD/2
SA0–SA2	IN	—	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to VDDSPD to act as a pullup on the system board.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board.
EVENT_n	Output (Open Drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on the TS/SPD part.
NC(TEST)			Used by memory bus analysis tools (unused (NC) on memory module)
NC			Not connected

Pin Configuration

Odd Row									
Pin#	**Symbol**	**Pin#**	**Symbol**	**Pin#**	**Symbol**	**Pin#**	**Symbol**	**Pin#**	**Symbol**
1	VSS	49	DQS2_t	97	CKE0	145	S1_n	193	DQ49
3	VSS	51	VSS	99	VDD	147	ODT1	195	VSS
5	DQ0	53	DQ18	101	BA2	149	VDD	197	DQS6_c
7	DQ1	55	DQ19	103	VDD	151	NC (S3_n)	199	DQS6_t
9	VSS	57	VSS	105	A11	153	VSS	201	VSS
11	DQS0_c	59	DQ24	107	A7	155	DQ32	203	DQ50
13	DQS0_t	61	DQ25	109	VDD	157	DQ33	205	DQ51
15	VSS	63	VSS	111	A5	159	VSS	207	VSS
17	DQ2	65	DQS3_c	113	A4	161	DQS4_c	209	DQ56
19	DQ3	67	DQS3_t	115	VDD	163	DQS4_t	211	DQ57
21	VSS	69	VSS	117	A2	165	VSS	213	VSS
23	DQ8	71	DQ26	119	VDD	167	DQ34	215	DQS7_c
25	DQ9	73	DQ27	121	CK1_t	169	DQ35	217	DQS7_t
27	VSS	75	VSS	123	CK1_n	171	VSS	219	VSS
29	DQS1_c	77	CB0	125	VDD	173	DQ40	221	DQ58
31	DQS1_t	79	CB1	127	VREFCA	175	DQ41	223	DQ59
33	VSS	81	VSS	129	NC (PAR_IN)	177	VSS	225	VSS
35	DQ10	83	DQS8_c	131	VDD	179	DQS5_c	227	SA2
37	DQ11	85	DQS8_t	133	A10/AP	181	DQS5_t	229	VSS
39	VSS	87	VSS	135	BA0	183	VSS	231	NC (SATA_RX_p)
41	DQ16	89	CB2	137	VDD	185	DQ42	233	NC (SATA_RX_n)
43	DQ17	91	CB3	139	WE_n	187	DQ43	235	VSS
45	VSS	93	VSS	141	CAS_n	189	VSS	237	VTT
47	DQS2_c	95	VTT	143	VDD	191	DQ48	239	VTT

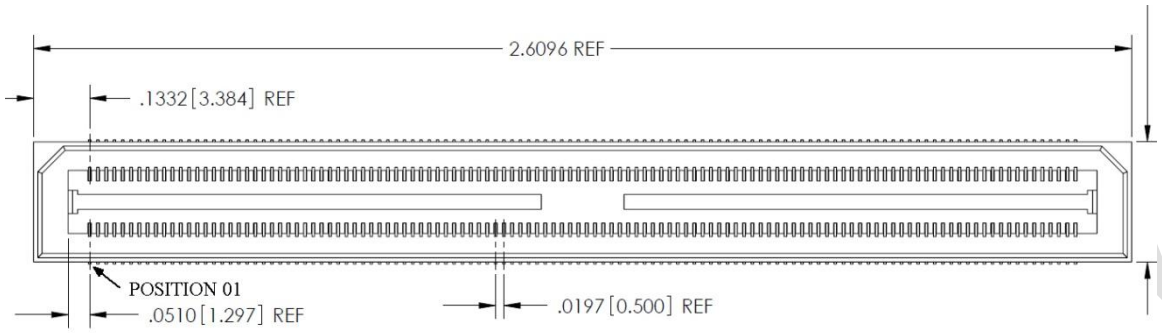
Even Row									
Pin#	**Symbol**	**Pin#**	**Symbol**	**Pin#**	**Symbol**	**Pin#**	**Symbol**	**Pin#**	**Symbol**
2	VSS	50	DM2	98	CKE1	146	VDD	194	VSS
4	VSS	52	VSS	100	VDD	148	ODT0	196	DM6
6	DQ4	54	DQ22	102	A15	150	A13	198	VSS
8	DQ5	56	DQ23	104	A14	152	VDD	200	DQ54
10	VSS	58	VSS	106	VDD	154	NC (S2_n)	202	DQ55
12	DM0	60	DQ28	108	A12/BC	156	VSS	204	VSS
14	VSS	62	DQ29	110	A9	158	DQ36	206	DQ60
16	DQ6	64	VSS	112	VDD	160	DQ37	208	DQ61
18	DQ7	66	DM3	114	A8	162	VSS	210	VSS
20	VSS	68	VSS	116	A6	164	DM4	212	DM7
22	DQ12	70	DQ30	118	VDD	166	VSS	214	VSS
24	DQ13	72	DQ31	120	A3	168	DQ38	216	DQ62
26	VSS	74	VSS	122	A1	170	DQ39	218	DQ63
28	DM1	76	CB4	124	VDD	172	VSS	220	VSS
30	VSS	78	CB5	126	CK0_t	174	DQ44	222	VDDSPD
32	DQ14	80	VSS	128	CK0_c	176	DQ45	224	SA0
34	DQ15	82	DM8	130	VDD	178	VSS	226	SA1
36	VSS	84	VSS	132	EVENT_n	180	DM5	228	SCL
38	DQ20	86	CB6	134	A0	182	VSS	230	SDA
40	DQ21	88	CB7	136	VDD	184	DQ46	232	VSS
42	VSS	90	VSS	138	BA1	186	DQ47	234	NC (SATA_TX_n)
44	VREFDQ	92	RESET_n	140	VDD	188	VSS	236	NC (SATA_TX_p)
46	NC (TEST)	94	NC (ERR_OUT_n)	142	RAS_n	190	DQ52	238	VSS
48	VSS	96	VTT	144	S0_n	192	DQ53	240	VTT

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

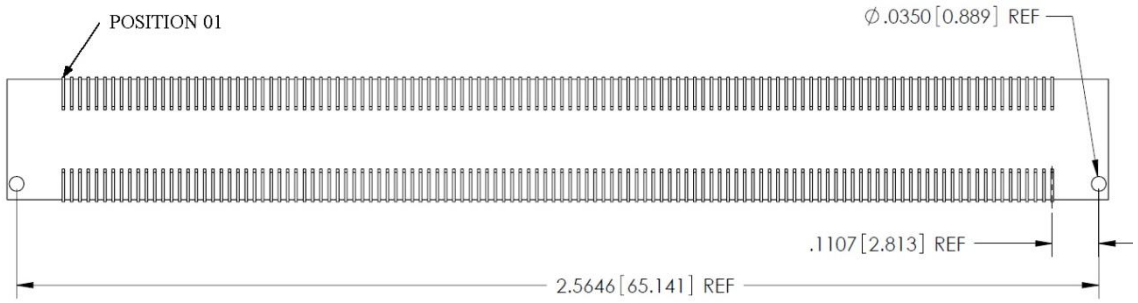
Mechanical Specifications

Connector on Memory Module (BSH-120-01-X-D-A)

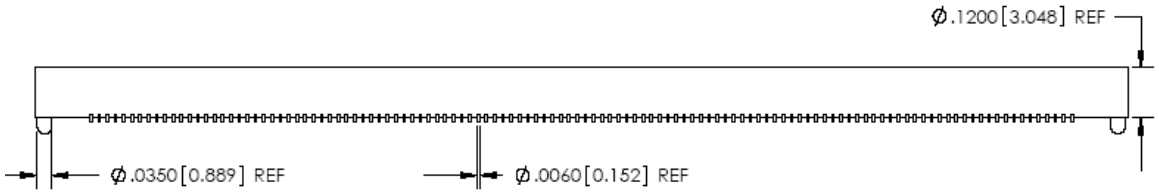
Top view:



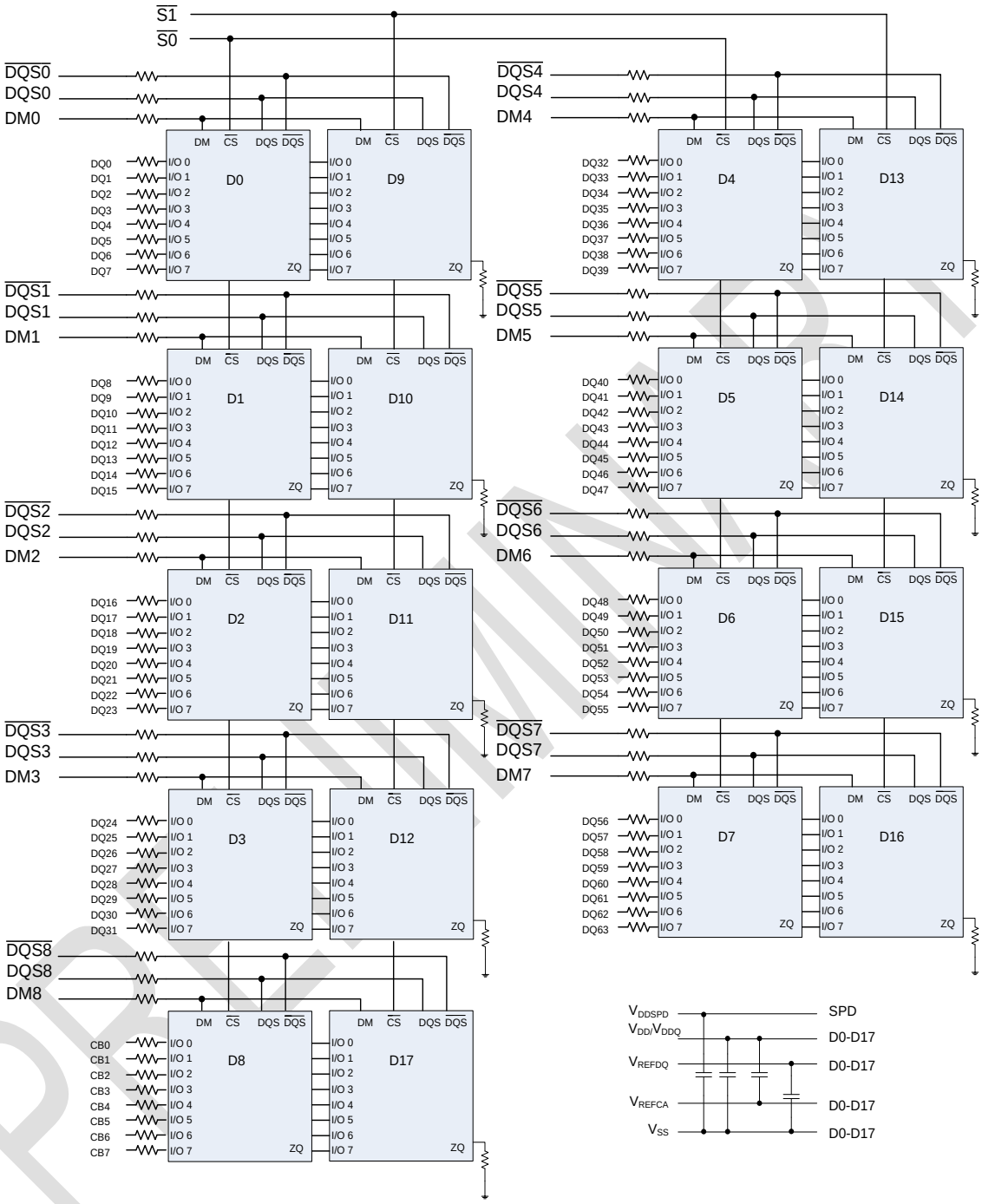
Bottom view:



Front view:



FUNCTIONAL BLOCK DIAGRAMM 8GB DDR3 SDRAM XR-DIMM, 2 RANK AND 18 COMPONENTS



BA0-BA2 → BA0-BA2: SDRAM D0-D17
A0-A15 → A0-A15: SDRAM D0-D17
$\overline{RAS}$ → $\overline{RAS}$: SDRAM D0-D17
$\overline{CAS}$ → $\overline{CAS}$: SDRAM D0-D17
$\overline{WE}$ → $\overline{WE}$: SDRAM D0-D17
ODT0 → ODT: SDRAM D0-D8
ODT1 → ODT: SDRAM D9-D17
CKE0 → CKE: SDRAM D0-D8
CKE1 → CKE: SDRAM D9-D17
CK0,CK1 → CK: SDRAM D0-D17
$\overline{CK0}$,$\overline{CK1}$ → $\overline{CK}$: SDRAM D0-D17
$\overline{RESET}$ → $\overline{RESET}$: SDRAM D0-D17

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationship must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDED document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-0.4	1.975	V
I/O Supply Voltage	V_{DDQ}	-0.4	1.975	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	I_I			µA
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-5	5	µA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-8	8	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	0.49 x V_{DDQ}-20mV	0.50 x V_{DDQ}	0.51x V_{DDQ}+20mV	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1		V_{DDQ} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.1	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.175	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.175	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. DDR3 modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

Parameter & Test Condition		Symbol	max. 12800-CL11	max. 10600-CL9	Unit
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	540	495	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	630	585	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast Exit	270 270	270	504	mA
	Slow Exit		270	288	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	360	360	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	450	450	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF} (always fast exit)		I_{DD3P}	360	360	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	540	540	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	1035	900	mA

Parameter & Test Condition	Symbol	max.		Unit
		12800-CL11	10600-CL9	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	1125	945	mA
BURST REFRESH CURRENT: $t_{CK} = t_{CK}$ (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	2610	2610	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	270	270	mA
OPERATING CURRENT *) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RRD} = t_{RRD}$ (I_{DD}), $t_{RCD} = t_{RCD}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	1710	1665	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS			
SYMBOL	**12800-CL11**	**10600-CL9**	**Unit**
CL (I_{DD})	11	9	t_{CK}
t_{RCD} (I_{DD})	13.75	13.5	ns
t_{RC} (I_{DD})	48.75	49.5	ns
t_{RRD} (I_{DD})	6	6	ns
t_{CK} (I_{DD})	1.25	1.5	ns
t_{RAS} MIN (I_{DD})	35	36	ns
t_{RAS} MAX (I_{DD})	70'200	70'200	ns
t_{RP} (I_{DD})	13.75	13.5	ns
t_{RFC} (I_{DD})	160	160	ns

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS			12800-CL11		10600-CL9		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Clock cycle time	CL = 11	t_{CK} (11)	1.25	-	-	-	ns
	CL = 10	t_{CK} (10)	1.5	<1.875	1.5	<1.875	
	CL = 9	t_{CK} (9)	1.5	<1.875	1.5	<1.875	
	CL = 8	t_{CK} (8)	1.875	<2.5	1.875	<2.5	
	CL = 7	t_{CK} (7)	1.875	<2.5	1.875	<2.5	
	CL = 6	t_{CK} (6)	2.5	3.3	2.5	3.3	
	CL = 5	t_{CK} (5)	3.0	3.3	3.0	3.3	
Internal READ command to first data		t_{AA}	13.75	-	13.5	-	
CK high-level width		$t_{CH\ (AVG)}$	0.47	0.53	0.47	0.53	t_{CK}
CK low-level width		$t_{CL\ (AVG)}$	0.47	0.53	0.47	0.53	t_{CK}
Data-out high-impedance window from CK/CK#		t_{HZ}	-	225	-	250	ps
Data-out low-impedance window from CK/CK#		t_{LZ}	-450	225	-500	250	ps
DQ and DM input setup time relative to DQS V_{REF}=1V/ns		t_{DS1V}	160	-	180	-	ps
DQ and DM input hold time relative to DQS V_{REF}=1V/ns		t_{DH1V}	145	-	165	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	360	-	400	-	ps
DQS, DQS# to DQ skew, per access		t_{DQSQ}	-	100	-	125	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	0.38	-	0.38	-	$t_{CK\ (AVG)}$
DQS input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}
DQS input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}
DQS, DQS# rising to/from CK, CK#		t_{DQSCK}	-225	225	-255	255	ps
DQS, DQS# rising to/from CK, CK# when DLL disabled		$t_{DQSCK\ DLL\ DIS}$	1	10	1	10	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.18	-	0.2	-	t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.18	-	0.2	-	t_{CK}
DQS read preamble		t_{RPRE}	0.9	Note1	0.9	Note1	t_{CK}
DQS read postamble		t_{RPST}	0.3	Note2	0.3	Note2	t_{CK}
DQS write preamble		t_{WPRE}	0.9	-	0.9	-	t_{CK}
DQS write postamble		t_{WPST}	0.3	-	0.3	-	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.27	+ 0.27	- 0.25	+ 0.25	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	560	-	620	-	ps
CTRL, CMD, Addr setup to CK, CK#		$t_{IS(Base)}$	45	-	65	-	ps
CTRL, CMD, Addr setup to CK, CK#	V_{REF} @ 1V/ns	$t_{IS(1V)}$	220	-	240	-	ps

1 The maximum preamble is bound by tLZDQS (MAX)

2 The maximum postamble is bound by tHZDQS (MAX)

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

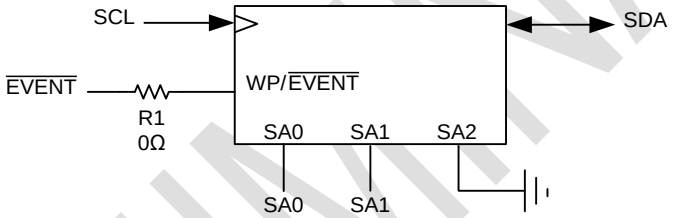
AC CHARACTERISTICS			12800-CL11		10600-CL9		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
CTRL, CMD, Addr hold to CK, CK#		$t_{IH(Base)}$	120	-	140	-	ps
CTRL, CMD, Addr hold to CK, CK# V_{REF} @ 1V/ns		$t_{IH(1V)}$	220	-	240	-	ps
CAS# to CAS# command delay		t_{CCD}	4	-	4	-	t_{CK}
ACTIVE to ACTIVE (same bank) command period		t_{RC}	48.75	-	49.5	-	ns
ACTIVE to ACTIVE minimum command period		t_{RRD}	max 4nCK,6ns	-	max 4nCK,6ns	-	ns
ACTIVE to READ or WRITE delay		t_{RCD}	13.75	-	13.5	-	ns
Four bank Activate period	1K Page size	t_{FAW}	30	-	30	-	ns
	2K Page size		40	-	45	-	
ACTIVE to PRECHARGE command		t_{RAS}	35	70’200	36	70’200	ns
Internal READ to precharge command delay		t_{RTP}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
Write recovery time		t_{WR}	15	-	15	-	ns
Auto precharge write recovery + precharge time		t_{DAL}	$t_{WR} + t_{RP}/t_{CK}$	-	$t_{WR} + t_{RP}/t_{CK}$	-	ns
Internal WRITE to READ command delay		t_{WTR}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
PRECHARGE command period		t_{RP}	13.75	-	13.5	-	ns
LOAD MODE command cycle time		t_{MRD}	4	-	4	-	t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval		t_{RFC}	260	70’200	260	70’200	ns
Average periodic refresh interval 0 °C ≤ T_{CASE} ≤ 85°C		t_{REFI}	-	7.8	-	7.8	µs
85 °C < T_{CASE} ≤ 95°C		$t_{REFI\ (IT)}$	-	3.9	-	3.9	
RTT turn-on from ODTL on reference		t_{AON}	-225	225	-250	250	ps
RTT turn-on from ODTL off reference		t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)		t_{AONPD}	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)		t_{AOFPD}	2	8,5	2	8,5	ns
RTT dynamic change skew		t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
Exit self refresh to commands not requiring a locked DLL		t_{XS}	max 5nCK,tRFC + 10ns	-	max 5nCK,tRFC + 10ns	-	ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		t_{WLS}	165	-	195	-	ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing		t_{WLH}	165	-	195	-	ps
First DQS, DQS# rising edge		t_{WLMRD}	40	-	40	-	t_{CK}
DQS, DQS# delay		$t_{WLDQSEN}$	25	-	25	-	t_{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800-CL11		10600-CL9		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Exit reset from CKE HIGH to a valid command	t_{XPR}	max 5nCK, t_{RFC} + 10ns	-	max 5nCK, t_{RFC} + 10ns	-	t_{CK}
Begin power supply ramp to power supplies stable	t_{VDDPR}	-	200	-	200	ms
RESET# LOW to power supplies stable	t_{RPS}	0	200	0	200	ms
RESET# LOW to I/O and RTT High-Z	t_{IOz}	-	20	-	20	ns
Exit precharge power-down to any non-READ command	t_{XP}	max 3nCK,6ns	-	max 3nCK,6ns	-	t_{CK}
CKE minimum high/low time	t_{CKE}	max 3nCK, 5ns	-	max 3nCK, 5.625ns	-	t_{CK}

Temperature Sensor with Serial Presence-Detect EEPROM



Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter / Condition	Symbol	MIN	MAX	Unit
Supply voltage	V_{DDSPD}	+3	+3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	+1.45	V_{DDSPD} +1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	-	550	mV
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	-	400	mV
Input current	I_{IN}	-5.0	5.0	µA
Temperature sensing range		TBD	TBD	°C
Temperature sensor accuracy		TBD	TBD	°C

A.C. Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Symbol	Parameter / Condition	MIN	MAX	Unit
f_{SCL}	SCL clock frequency	10	400	kHz
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
t_F	SDA fall time		300	ns
t_R	SDA rise time		300	ns
$t_{HD:DAT}$	Data hold time (accepted for Input Data)	0		ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
$t_{H:STA}$	Start condition hold time	600		ns
t_{HIGH}	High Period of SCL	600		ns
t_{LOW}	Low Period of SCL	1300		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	Start condition setup time	600		ns
$t_{SU:STO}$	Stop condition setup time	600		ns
$t_{TIMEOUT}$	SMBus SCL Clock Low Timeout	25	35	ms
t_I	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU}	Power-up Delay to Valid Temperature Recording		100	ms

Temperature Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Parameter	Test Conditions/Comments	MAX	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T_A ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	°C
	-40°C ≤ T_A ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Conversion Time		100	Ms
Thermal Resistance[1] θ_{JA}	Junction-to-Ambient (Still Air)	92	°C/W

[1] Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where TJ is the junction temperature and TA is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

Slave Address Bits of Temperature Sensor

Device	Device Type Identifier				Select Address Signals			R/W#
	b7[1]	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/W#
Temp. Sensor	0	0	1	1	A_2	A_1	A_0	R/W#

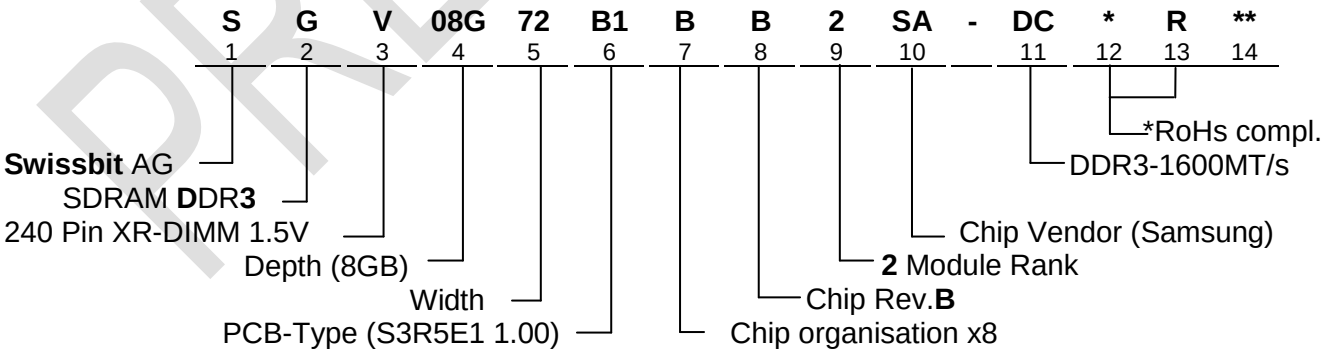
[1] The most significant bit, b7, is sent first.

SERIAL PRESENCE-DETECT MATRIX

Byte	Byte Description	12800-CL11	10600-CL9
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISON	0x11	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x08	
4	SDRAM DEVICE DENSITY & BANKS	0x04	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x21	
6	BYTE 6 RESERVED	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x09 0x01	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x11	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ($t_{CK\ MIN}$)	0x0A	0x0C
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0xFE	0x7E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ($t_{AA\ MIN}$)	0x69	
17	MIN WRITE RECOVERY TIME ($t_{WR\ MIN}$)	0x78	
18	MIN RAS# TO CAS# DELAY ($t_{RCD\ MIN}$)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ($t_{RRD\ MIN}$)	0x30	0x30
20	MIN ROW PRECHARGE DELAY ($t_{RP\ MIN}$)	0x69	
21	UPPER NIBBLE FOR t_{RAS} & t_{RC}	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ($t_{RAS\ MIN}$)	0x18	0x20
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY ($t_{RC\ MIN}$)	0x81	0x89
24	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) LSB	0x20	
25	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) MSB	0x08	
26	MIN INTERNAL WRITE TO READ CMD DELAY ($t_{WTR\ MIN}$)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ($t_{RTP\ MIN}$)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) MSB	0x00	0x00
29	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) LSB	0xF0	0xF0
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x83	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x05	

Byte	Byte Description	12800-CL11	10600-CL9
32	Module Thermal Sensor	0x80	
33-59	BYTES 32-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x18	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x1F	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x00	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0x2194	tbd
128-145	MODULE PART NUMBER	"SGV08G72B1BB2SA-xx"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	X	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0xCE	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xFF	

Part Number Code



* optional / additional information
**T=Thermal Sensor

Revision History		
Revision	Changes	Date
0.8	Initial Revision	21.06.2012

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