# 2N3771, 2N3772

# High Power NPN Silicon Power Transistors

These devices are designed for linear amplifiers, series pass regulators, and inductive switching applications.

### Features

- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 3.75 Adc @ $V_{CE}$ = 40 Vdc − 2N3771
  = 2.5 Adc @ $V_{CE}$ = 60 Vdc − 2N3772
- These Devices are Pb−Free and are RoHS Compliant

**MAXIMUM RATINGS** (Note 1)

| Rating | Symbol | 2N3771 | 2N3772 | Unit |
|---|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | 40 | 60 | Vdc |
| Collector−Emitter Voltage | $V_{CEX}$ | 50 | 80 | Vdc |
| Collector−Base Voltage | $V_{CB}$ | 50 | 100 | Vdc |
| Emitter−Base Voltage | $V_{EB}$ | 5.0 | 7.0 | Vdc |
| Collector Current − Continuous<br>Peak | $I_C$ | 30<br>30 | 20<br>30 | Adc |
| Base Current − Continuous<br>Peak | $I_B$ | 7.5<br>15 | 5.0<br>15 | Adc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 150<br>0.855 | | W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −65 to +200 | | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Case | $\theta_{JC}$ | 1.17 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

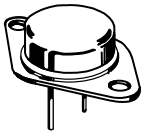
1. Indicates JEDEC registered data.

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**20 and 30 AMPERE POWER TRANSISTORS NPN SILICON 40 and 60 VOLTS, 150 WATTS**

**MARKING DIAGRAM**



**TO−204AA (TO−3)**
**CASE 1−07**
**STYLE 1**




2N377x = Device Code
x = 1 or 2
G = Pb−Free Package
A = Assembly Location
YY = Year
WW = Work Week
MEX = Country of Origin

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| 2N3771G | TO−204 (Pb−Free) | 100 Units / Tray |
| 2N3772G | TO−204 (Pb−Free) | 100 Units / Tray |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Emitter Sustaining Voltage (Note 2 and 3)<br>($I_C$ = 0.2 Adc, $I_B$ = 0) | 2N3771<br>2N3772 | $V_{CEO(sus)}$ | 40<br>60 | –<br>– | Vdc |
| Collector−Emitter Sustaining Voltage<br>($I_C$ = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, $R_{BE}$ = 100 Ω) | 2N3771<br>2N3772 | $V_{CEX(sus)}$ | 50<br>80 | –<br>– | Vdc |
| Collector−Emitter Sustaining Voltage<br>($I_C$ = 0.2 Adc, $R_{BE}$ = 100 Ω) | 2N3771<br>2N3772 | $V_{CER(sus)}$ | 45<br>70 | –<br>– | Vdc |
| Collector Cutoff Current (Note 2)<br>($V_{CE}$ = 30 Vdc, $I_B$ = 0)<br>($V_{CE}$ = 50 Vdc, $I_B$ = 0)<br>($V_{CE}$ = 25 Vdc, $I_B$ = 0) | <br>2N3771<br>2N3772 | $I_{CEO}$ | <br>–<br>– | <br>10<br>10 | mAdc |
| Collector Cutoff Current (Note 2)<br>($V_{CE}$ = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc)<br>($V_{CE}$ = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)<br>($V_{CE}$ = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)<br>($V_{CE}$ = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, $T_C$ = 150°C)<br>($V_{CE}$ = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, $T_C$ = 150°C) | <br>2N3771<br>2N3772<br>2N6257<br>2N3771<br>2N3772 | $I_{CEV}$ | <br>–<br>–<br>–<br>–<br>– | <br>2.0<br>5.0<br>4.0<br>10<br>10 | mAdc |
| Collector Cutoff Current (Note 2)<br>($V_{CB}$ = 50 Vdc, $I_E$ = 0)<br>($V_{CB}$ = 100 Vdc, $I_E$ = 0) | <br>2N3771<br>2N3772 | $I_{CBO}$ | <br>–<br>– | <br>2.0<br>5.0 | mAdc |
| Emitter Cutoff Current (Note 2)<br>($V_{BE}$ = 5.0 Vdc, $I_C$ = 0)<br>($V_{BE}$ = 7.0 Vdc, $I_C$ = 0) | <br>2N3771<br>2N3772 | $I_{EBO}$ | <br>–<br>– | <br>5.0<br>5.0 | mAdc |
| **ON CHARACTERISTICS** (Note 2) | | | | | |
| DC Current Gain (Note 3)<br>($I_C$ = 15 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 10 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 8.0 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 30 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 20 Adc, $V_{CE}$ = 4.0 Vdc) | <br>2N3771<br>2N3772<br><br>2N3771<br>2N3772 | $h_{FE}$ | <br>15<br>15<br><br>5.0<br>5.0 | <br>60<br>60<br><br>–<br>– | – |
| Collector−Emitter Saturation Voltage<br>($I_C$ = 15 Adc, $I_B$ = 1.5 Adc)<br>($I_C$ = 10 Adc, $I_B$ = 1.0 Adc)<br>($I_C$ = 30 Adc, $I_B$ = 6.0 Adc)<br>($I_C$ = 20 Adc, $I_B$ = 4.0 Adc) | <br>2N3771<br>2N3772<br>2N3771<br>2N3772 | $V_{CE(sat)}$ | <br>–<br>–<br>–<br>– | <br>2.0<br>1.4<br>4.0<br>4.0 | Vdc |
| Base−Emitter On Voltage<br>($I_C$ = 15 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 10 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 8.0 Adc, $V_{CE}$ = 4.0 Vdc) | <br>2N3771<br>2N3772 | $V_{BE(on)}$ | <br>–<br>– | <br>2.7<br>2.2 | Vdc |
| ***DYNAMIC CHARACTERISTICS** (Note 2) | | | | | |
| Current−Gain — Bandwidth Product<br>($I_C$ = 1.0 Adc, $V_{CE}$ = 4.0 Vdc, $f_{test}$ = 50 kHz) | | $f_T$ | 0.2 | – | MHz |
| Small−Signal Current Gain<br>($I_C$ = 1.0 Adc, $V_{CE}$ = 4.0 Vdc, f = 1.0 kHz) | | $h_{fe}$ | 40 | – | – |
| **SECOND BREAKDOWN** | | | | | |
| Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non−repetitive)<br>($V_{CE}$ = 40 Vdc)<br>($V_{CE}$ = 60 Vdc) | <br>2N3771<br>2N3772 | $I_{S/b}$ | <br>3.75<br>2.5 | <br>–<br>– | Adc |

2. Indicates JEDEC registered data.
3. Pulse Test: 300 μs, Rep. Rate 60 cps.

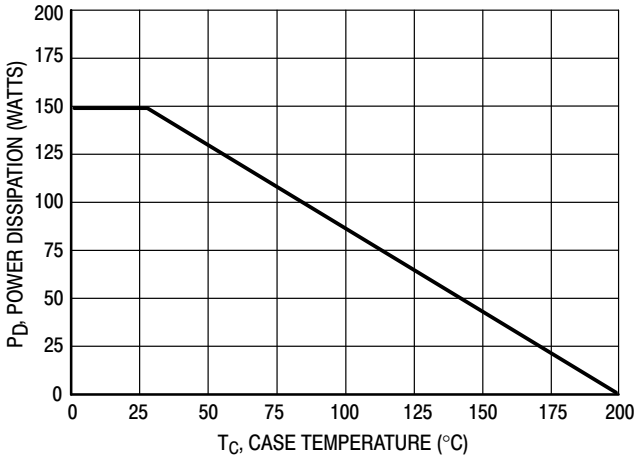



**Figure 1. Power Derating**

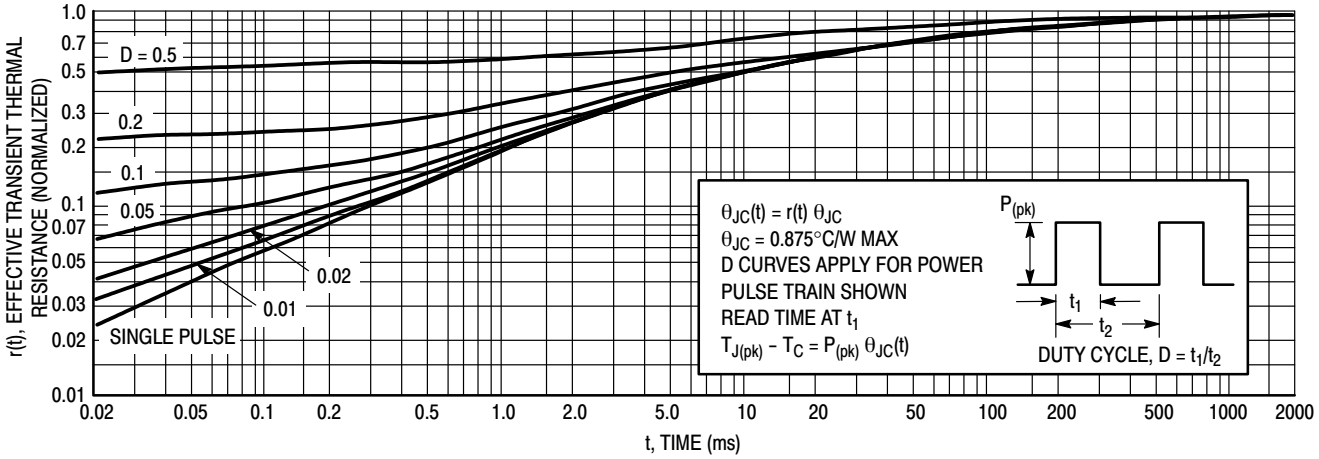



**Figure 2. Thermal Response — 2N3771, 2N3772**

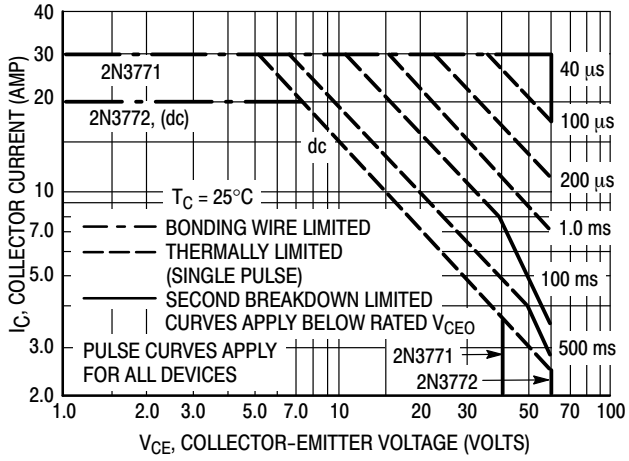



**Figure 3. Active−Region Safe Operating Area — 2N3771, 2N3772**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

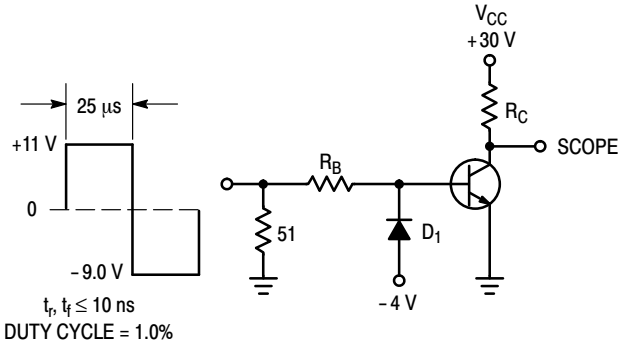



**Figure 4. Switching Time Test Circuit**

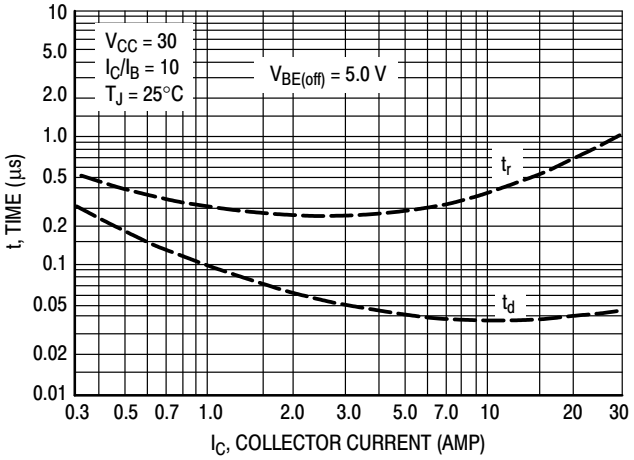



**Figure 5. Turn−On Time**

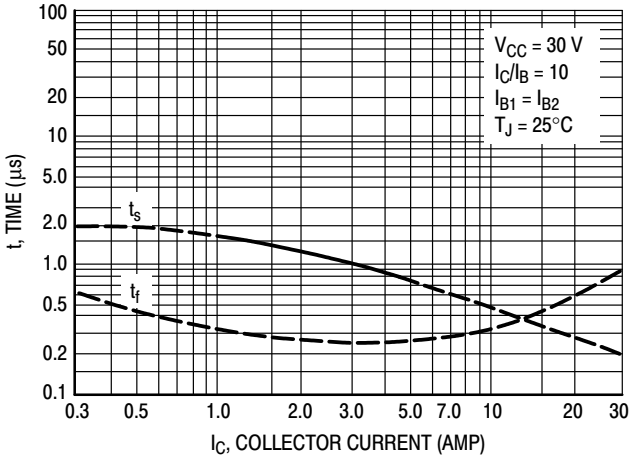



**Figure 6. Turn−Off Time**

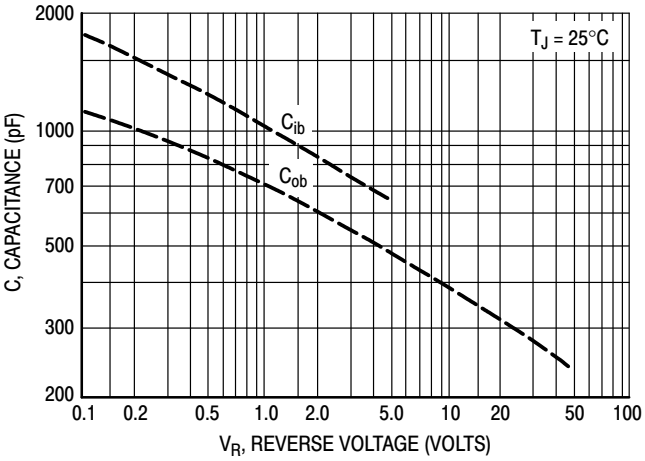



**Figure 7. Capacitance**

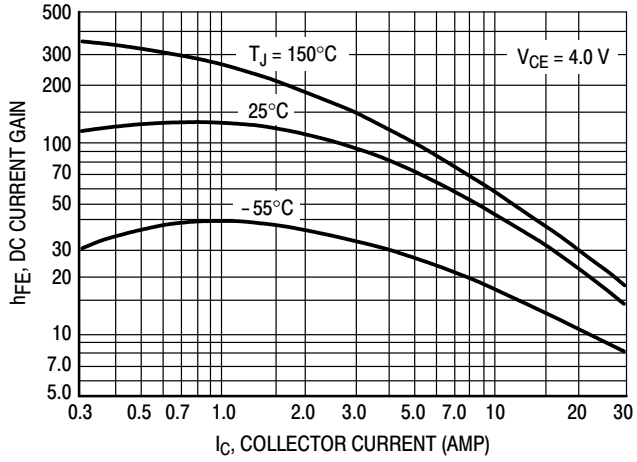



**Figure 8. DC Current Gain**

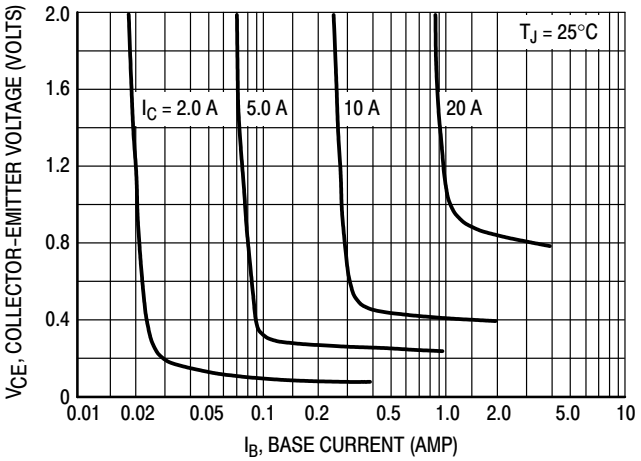
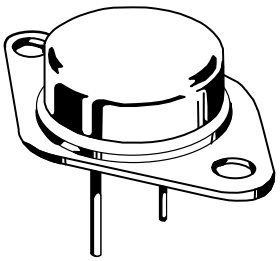


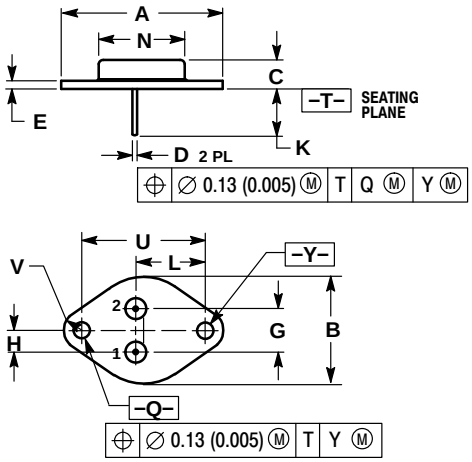

**Figure 9. Collector Saturation Region**



**SCALE 1:1**

**TO−204 (TO−3)**
**CASE 1−07**
**ISSUE Z**

**DATE 05/18/1988**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.550 REF | | 39.37 REF | |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC | | 10.92 BSC | |
| H | 0.215 BSC | | 5.46 BSC | |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC | | 16.89 BSC | |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | | 30.15 BSC | |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

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