Power Management Integrated Circuit (PMIC) for i.MX50/53 Families

34708

POWER MANAGEMENT

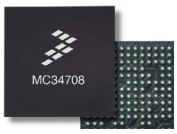
The MC34708 is the Power Management Integrated Circuit (PMIC) designed specifically for use with the Freescale i.MX50 and i.MX53 families. This device is powered by SMARTMOS technology.

Features

- Six multi-mode buck regulators for direct supply of the processor core, memory, and peripherals
- Boost regulator for USB OTG support
- Eight regulators with internal and external pass devices for thermal budget optimization
- USB/UART/Audio switching for mini-micro USB connector
- 10-bit ADC for monitoring battery and other inputs
- Real time clock and crystal oscillator circuitry with coin cell backup/ charger
- SPI/I^{2}C bus for control and register interface



VK SUFFIX (PB-FREE)
98ASA00312D
206 MAPBGA
8.0 X 8.0 (0.5 MM PITCH)



VM SUFFIX (PB-FREE)
98ASA00299D
206 MAPBGA
13.0 X 13.0 (0.8 MM PITCH)

Applications
Tablets
Smart Mobile Devices
Portable Navigation Devices

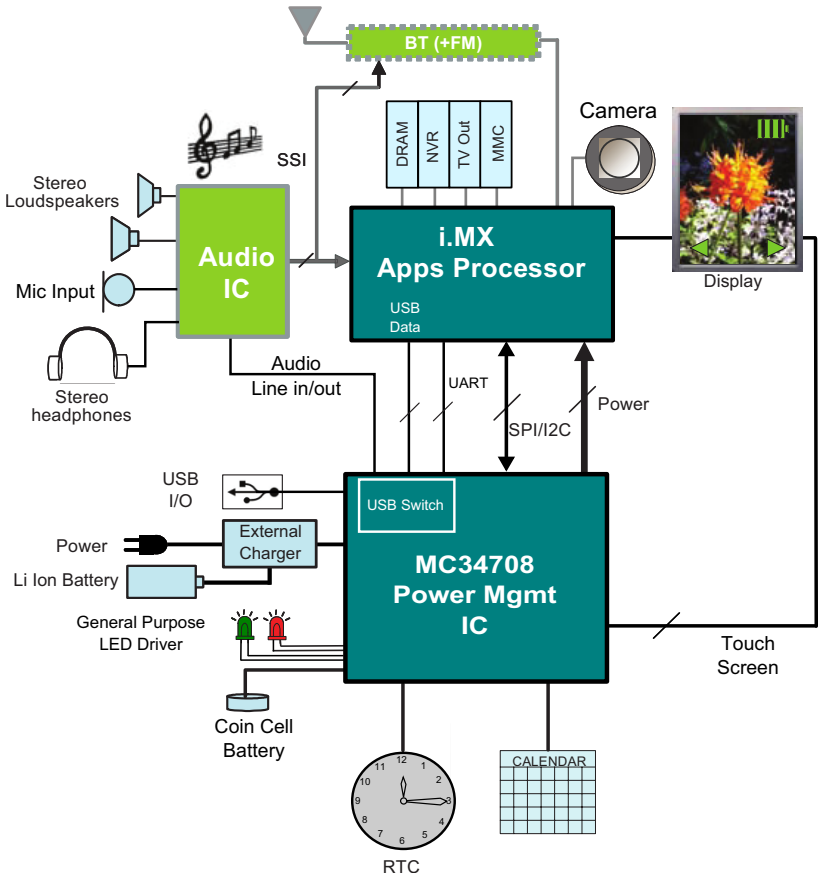


Figure 1. MC34708 Simplified Application Diagram

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1 Orderable Parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

Part Number [1]	Temperature (T_A)	Package
MC34708VK	-40 to 85 °C	206 MAPBGA - 8.0 x 8.0 mm - 0.5 mm pitch
MC34708VM		206 MAPBGA - 13 x 13 mm - 0.8 mm pitch

Notes
1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

2 Part Identification

This section provides an explanation of the part numbers and their alpha numeric breakdown.

2.1 Description

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

2.2 Format and Examples

Part numbers for a given device have the following format, followed by a device example:

Table 2 - Part Numbering - Analog:

MC tt xxx r v PP RR - MC34708VKR2

2.3 Fields

These tables list the possible values for each field in the part number (not all combinations are valid).

Table 2: Part Numbering - Analog

FIELD	DESCRIPTION	VALUES
MC	Product Category	• MC- Qualified Standard • PC- Prototype Device
tt	Temperature Range	• 34 = -40 °C to ≤ 105 °C
xxx	Product Number	• Assigned by Marketing
r	Revision	• (default blank)
v	Variation	• (default blank)
PP	Package Identifier	• Varies by package
RR	Tape and Reel Indicator	• R2 = 13 inch reel hub size

3 Internal Block Diagram

3.1 Simplified Internal Diagram

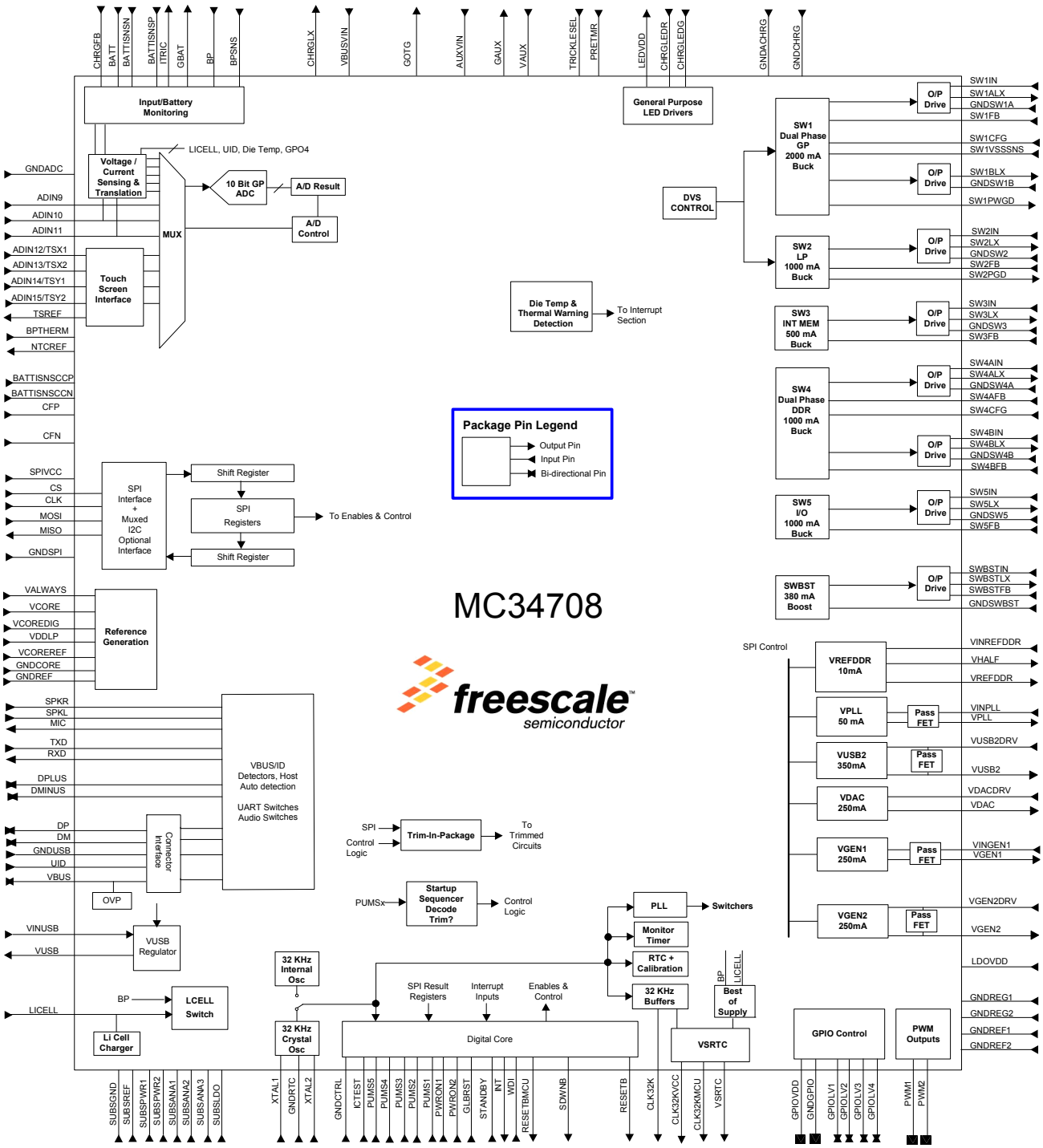


Figure 2. Simplified Internal Block Diagram

4 Pin Connections

4.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		TRICKLESEL	GNDACHRG	BATT	CFP	BP	VBUSVIN	CHRGLX	GNDCHRG	LEDVDD	LICELL	PWM1	GPIOVDD	PUMS4	
B	AUXVIN	AUXVIN	PRETMR	BPTHERM	CFN	GBAT	VBUSVIN	CHRGLX	GNDCHRG	CHRGLEDG	GPIOLV1	GNDGPIO	PUMS3	PUMS2	SUBSANA2
C	AUXVIN	AUXVIN	SUBSANA3	NTCREF	CHRGFB	BPSNS	VBUSVIN	CHRGLX	GNDCHRG	PWM2	GPIOLV3	PUMS1	GNDSW2	GNDSW2	GNDSW2
D	VAUX	GOTG	GAUX	SDWNB			VBUSVIN	CHRGLX	GNDCHRG	ICTEST	GPIOLV2	PUMS5	SW2LX	SW2LX	SW2LX
E	RESETB	GNDCTRL	PWRON2	INT		BATTISNSCCN	BATTISNSP	ITRIC	SUBSPWR1	CHRGLEDR	GPIOLV0	SW2FB	SW2IN	SW2IN	SW2IN
F	MISO	GNDSPI	MOSI	SPIVCC	RESETBMCU	BATTISNSCCP	BATTISNSN	SUBSPWR1	SUBSPWR1		GNDREF2	SWBSTIN	SWBSTIN	GNDSW3	GNDSW3
G	CLK	CS	VINUSB	RXD	TXD		GLBRST	PWRON1	SUBSPWR1	SW2PWGD	SW3FB	GNDSWBST	GNDSWBST	SW3LX	SW3LX
H	VBUS	VUSB	UID	VALWAYS	SUBSREF	SUBSPWR1	MIC	SUBSPWR1	SUBSPWR1	CLK32KMCU	CLK32KVCC	SWBSTFB	CLK32K	SW3IN	SW3IN
J	DM	SPKR	VCOREDIG	VDDLP	STANDBY	TSY2	TSY1	SUBSPWR1	SUBSPWR1	VDACDRV	VINPLL	VPLL	VSRTC	SWBSTLX	SWBSTLX
K	DP	SPKL	VCORE	TSX1		ADIN10	ADIN9	SUBSPWR1	SUBSPWR1	VHALF	VGEN2	VDAC	GNDREG1	GNDRTC	SUBSLDO
L	DPLUS	GNDCORE	GNDUSB	WDI	TSX2	ADIN11	SUBSPWR1	GNDREF1	SW1VSSSNS	SW1CFG	VINREFDDR	GNDREG2	VUSB2	LDOVDD	XTAL2
M	DMINUS	GNDREF				SW4CFG	SW5FB			SW1FB	SW1PWGD		VGEN1	VUSB2DRV	XTAL1
N	VCOREREF	GNDADC	GNDADC	GNDADC			SW5IN	SW5LX	GNDSW5		SW1IN	SW1IN	SUBSANA1	VINGEN1	VGEN2DRV
P	TSREF	GNDSW4A	GNDADC	GNDADC	SW4BFB	SW4AFB	SW5IN	SW5LX	GNDSW5	GNDSW1A	SW1ALX	SW1IN	SW1BLX	GNDSW1B	VREFDDR
R		SW4ALX	SW4AIN	SW4BIN	SW4BLX	GNDSW4B	SW5IN	SW5LX	GNDSW5	GNDSW1A	SW1ALX	SW1IN	SW1BLX	GNDSW1B	

Legend

- LDOs
- Switching Regulators
- Control Logic
- Misc
- RTC
- Ground
- USB
- ADC
- SPI/I2C
- No Connect
- No Ball

Figure 3. Top View Ballmap

4.2 Pin Definitions

Table 3. MC34708 Pin Definitions

Pin Number	Pin Name	Pin Function	Definition
Charger (Function no longer supported on MC34708)			
A7, B7, C7, D7	VBUSVIN	NC	Charger Not supported. No Connect
B1, B2, C1, C2	AUXVIN	NC	Charger Not supported. No Connect
D1	VAUX	NC	Charger Not supported. No Connect
A8, B8, C8, D8	CHRGLX	NC	Charger Not supported. No Connect
C5	CHRGFB	I	Connect to BATT pin
D2	GOTG	NC	Charger Not supported. No Connect
D3	GAUX	NC	Charger Not supported. No Connect
C6	BPSNS	I	BP sense point
A6	BP	I	1. Application supply point 2. Input supply to the IC core circuitry 3. Application supply voltage sense
B6	GBAT	O	Connect to GND
E8	ITRIC	NC	Charger Not supported. No Connect
E7	BATTISNSP	I	Battery current sensing point.(Optional) If required, connect a 20 mΩ sense resistor between BATTISNSP and BATTISNSN
F7	BATTISNSN	I	Battery current sensing point (Optional) If required, connect a 20 mΩ sense resistor between BATTISNSP and BATTISNSN
A4	BATT	I	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
F6	BATTISNSCCP	NC	Coulomb counter Not supported. No Connect
E6	BATTISNSCCN	NC	Coulomb counter Not supported. No Connect
A2	TRICKLESEL	I	Connect to VCOREDIG
B3	PRETMR	I	Connect to Ground
A5	CFP	NC	Coulomb Counter Not supported. No Connect
B5	CFN	NC	Coulomb Counter Not supported. No Connect
A10	LEDVDD	O	LED supply
E10	CHRGLEDR	I	Red LED driver

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
B10	CHRGLEDG	I	Green LED driver
A3	GNDACHRG	GND	Analog ground
A9, B9, C9, D9	GNDCHRG	GND	Ground
C4	NTCREF	NC	Charger Not supported. No Connect
B4	BPTHERM	I	Connect to Ground
IC Core			
K3	VCORE	O	Regulated supply for the IC analog core circuitry
J3	VCOREDIG	O	Regulated supply for the IC digital core circuitry
H4	VALWAYS	O	Always on supply for internal core circuitry
N1	VCOREREF	O	Main bandgap reference
J4	VDDLP	O	VDDLP reference
L2	GNDCORE	GND	Ground for the IC core circuitry
M2	GNDREF	GND	Ground reference for the IC core circuitry
Switching Regulators			
N11, N12, P12, R12	SW1IN	I	SW1 input
P11, R11	SW1ALX	O	SW1A switch node connection
M10	SW1FB	I	SW1 feedback
P10, R10	GNDSW1A	GND	Ground for SW1A
L9	SW1VSSSNS	GND	SW1 sense
M11	SW1PWGD	O	Powergood signal for SW1
P13, R13	SW1BLX	O	SW1B switch node connection
P14, R14	GNDSW1B	GND	Ground for SW1B
L10	SW1CFG	I	SW1A/B mode configuration
E13, E14, E15	SW2IN	I	SW2 input
D13, D14, D15	SW2LX	O	SW2 switch node connection
E12	SW2FB	I	SW2 feedback
C13, C14, C15	GNDSW2	GND	Ground for SW2
G10	SW2PWGD	O	Powergood signal for SW2
H14, H15	SW3IN	I	SW3 input
G14, G15	SW3LX	O	SW3 switch node connection
G11	SW3FB	I	SW3 feedback
F14, F15	GNDSW3	GND	Ground for SW3
F11	GNDREF2	GND	Ground reference for switching regulators
R3	SW4AIN	I	SW4A input

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
R2	SW4ALX	O	SW4A switch node connection
P6	SW4AFB	I	SW4A feedback
P2	GNDSW4A	GND	Ground for SW4A
R4	SW4BIN	I	SW4B input
R5	SW4BLX	O	SW4B switch node connection
P5	SW4BFB	I	SW4B feedback
R6	GNDSW4B	GND	Ground for SW4B
M6	SW4CFG	I	SW4A/B mode configuration
N7, P7, R7	SW5IN	I	SW5 input
N8, P8, R8	SW5LX	O	SW5 output
M7	SW5FB	I	SW5 feedback
N9, P9, R9	GNDSW5	GND	Ground for SW5
L8	GNDREF1	GND	Ground reference for Switching Regulators
F12, F13	SWBSTIN	I	Boost Regulator BP supply
J14, J15	SWBSTLX	O	SWBST switch node connection
H12	SWBSTFB	I	Boost Regulator feedback
G12, G13	GNDSWBST	GND	Ground for boost Regulator
LDO Regulators			
L11	VINREFDDR	I	VREFDDR input supply
P15	VREFDDR	O	VREFDDR regulator output
K10	VHALF	O	Half supply reference for VREFDDR
J11	VINPLL	I	VPLL input supply
J12	VPLL	O	VPLL regulator output
J10	VDACDRV	O	Drive output for VDAC regulator using external PNP device
K12	VDAC	O	VDAC regulator output
L14	LDOVDD	I	Supply pin for VUSB2, VDAC, and VGEN2. Must always be connected to the same supply as the PNP emitter. Recommended to use BP as the LDOVDD supply. See Figure 38 for a typical connection diagram.
M14	VUSB2DRV	I	1. VUSB2 input using internal PMOS FET
		O	2. Drive output for VUSB2 regulator using external PNP device
L13	VUSB2	O	VUSB2 regulator output
N14	VINGEN1	I	VGEN1 input supply
M13	VGEN1	O	VGEN1 regulator output
N15	VGEN2DRV	I	1. VGEN2 input using internal PMOS FET
		O	2. Drive output for VGEN2 regulator using external PNP device
K11	VGEN2	O	VGEN2 regulator output
J13	VSRTC	O	Output regulator for SRTC module on processor
K13	GNDREG1	GND	Ground for regulators 1

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
L12	GNDREG2	GND	Ground for regulators 2
A13	GPIOVDD	I	Supply for GPIO
E11	GPIOLV0	I/O	General purpose input/output 0
B11	GPIOLV1	I/O	General purpose input/output 1
D11	GPIOLV2	I/O	General purpose input/output 2
C11	GPIOLV3	I/O	General purpose input/output 3
A12	PWM1	O	PWM output 1
C10	PWM2	O	PWM output 2
B12	GNDGPIO	-	GPIO ground
Control Logic			
A11	LICELL	I/O	1. Coin cell supply input 2. Coin cell charger output
M15	XTAL1	I	32.768 kHz Oscillator crystal connection 1
L15	XTAL2	I	32.768 kHz Oscillator crystal connection 2
K14	GNDRTC	GND	Ground for the RTC block
H11	CLK32KVCC	I	Supply voltage for 32 kHz buffer
H13	CLK32K	O	32 kHz Clock output for peripherals
H10	CLK32KMCU	O	32 kHz Clock output for processor
E1	RESETB	O	Reset output for peripherals
F5	RESETBMCU	O	Reset output for processor
L4	WDI	I	Watchdog input
J5	STANDBY	I	Standby input signal from processor
E4	INT	O	Interrupt to processor
G8	PWRON1	I	Power on/off button connection 1
E3	PWRON2	I	Power on/off button connection 2
G7	GLBRST	I	Global Reset
C12	PUMS1	I	Power up mode supply setting 1
B14	PUMS2	I	Power up mode supply setting 2
B13	PUMS3	I	Power up mode supply setting 3
A14	PUMS4	I	Power up mode supply setting 4
D12	PUMS5	I	Power up mode supply setting 5
D10	ICTEST	I	Connect to ground for normal mode operation.
E2	GNDCTRL	GND	Ground for control logic
F4	SPIVCC	I	Supply for SPI bus
G2	CS	I	Primary SPI select input
G1	CLK	I	Primary SPI clock input
F3	MOSI	I	Primary SPI write input
F1	MISO	O	Primary SPI read output

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
D4	SDWNB	O	Indication of imminent system shutdown
F2	GNDSPI	GND	Ground for SPI interface
USB [(2)]			
H3	UID	I/O	USB OTG transceiver cable ID
L3	GNDUSB	GND	USB Ground
K1	DP	I/O	USB Data +
J1	DM	I/O	USB Data –
L1	DPLUS	I/O	Processor D+
M1	DMINUS	I/O	Processor D-
G4	RXD	O	UART Receive
G5	TXD	I/O	UART Transmit
H7	MIC	O	Mic output
J2	SPKR	I	Speaker right
K2	SPKL	I	Speaker left
H1	VBUS	I/O	USB transceiver cable interface VBUS & OTG supply output
H2	VUSB	O	USB transceiver regulator output
G3	VINUSB	I	Input option for VUSB; tie to SWBST at top level.
A to D Converter			
K7	ADIN9	I	ADC generic input channel 9
K6	ADIN10	I	ADC generic input channel 10,
L6	ADIN11	I	ADC generic input channel 11
K4	TSX1/ADIN12	I	Touch Screen Interface X1 or ADC generic input channel 12
L5	TSX2/ADIN13	I	Touch Screen Interface X2 or ADC generic input channel 13
J7	TSY1/ADIN14	I	Touch Screen Interface Y1 or ADC generic input channel 14
J6	TSY2/ADIN15	I	Touch Screen Interface Y2 or ADC generic input channel 15
P1	TSREF	O	Touch Screen Reference
N2, N3, N4, P3, P4	GNDADC	GND	Ground for ADC
Thermal Grounds			
H5	SUBSREF	GND	Substrate ground connection for reference circuitry
E9, F8,F9, L7, G9, H6, H8, H9, J8, J9, K8, K9	SUBSPWR1	GND	Substrate ground connection for power devices SW1, SW4, SW5
K15	SUBSLDO	GND	Substrate ground connection for all LDOs
N13	SUBSANA1	GND	Substrate ground connection for analog circuitry of SW1, SW4, SW5
B15	SUBSANA2	GND	Substrate ground connection for analog circuitry of SW2, SW3, SWBST

Table 3. MC34708 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Definition
C3	SUBSANA3	GND	Substrate ground connection for analog circuitry

Notes

2. In applications without USB support, leave all USB pins unconnected.

5 General Product Characteristics

5.1 Maximum Ratings

Table 4. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Max.	Unit	Notes
ELECTRICAL RATINGS				
V_{BATT}, V_{BP}, V_{LICELL}	Input Supply Pins		V	
	• BATT, BP, BPSNS	4.8		
	• LICELL	4.8		
	Input Sense Pins		V	
	• CHRGFB	7.5		
	• BATTISNSP, BATTISNSN	5.5		
	LED Drivers Pins		V	
	• CHRGLEDR, CHRGLEDG	7.5		
	IC Core Reference		V	
	• VCOREREF	1.5		
	• VCOREDIG, VDDLP	1.65		
	• VCORE	3.6		
	• VALWAYS	7.5		
	Switching Regulators Pins		V	
	• SWxIN, SWxLX, SWBSTFB	5.5		
	• SWxFB, SWxPWGD, SWxCFG	3.6		
	• SWBSTLX	7.5		
	LDO Regulator Pins		V	
	• VREFDDR, VHALF	1.5		
	• VPLL, VGEN1, VINGEN1, VSRTC	2.5		
	• VINREFDDR,VDAC, VUSB2, VGEN2,	3.6		
	• VINPLL, VDACDRV, VUSB2DRV, VGEN2DRV	4.8		
	• LDOVDD	5.5		
	GPIO Pins		V	
	• GPIOVDD, GPIOLVx, PWMx	2.5		
	Control Logic Pins		V	
	• ICTEST	1.8		
	• XTAL1, XTAL2	2.5		
	• CLK32KVCC, CLK32K, CLK32KMCU, WDI, STANDBY,INT, PWRON1, PWRON2, GLBRST, PUMSx, SPIVCC, CS, CLK, MOSI, MISO, SDWNB	3.6		
	Mini/Micro USB Interface Pins		V	
	• VBUS input sense pin	20		
	• VUSB	3.6		
	• UID, DP, DM, DPLUS, DMINUS, RXD, TXD, MIC, SPKR, SPKL, VINUSB	5.5		
	ADC Interface Pins		V	
	• ADINx, TSX1/ADIN12, TSX2/ADIN13, TSY1/ADIN14, TSY2/ADIN15, TSREF	4.8		

Table 4. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Max.	Unit	Notes
V_{ESD}	ESD Ratings		V	
	• Human Body Model All pins	±2000		(3)
	• Charge Device Model All pins	±500		(3)
	• Air Gap Discharge Model for UID, VBUS, DP, and DM pins	±15000		(4)
	• Human Body Model (HBM) for UID, VBUS, DP, and DM pins	±8000		(4)

Notes

3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
4. Need external ESD protection diode array to meet IEC1000-4-2 15000 V Air Gap discharge and 8000 V HBM requirements. (CZAP = 150 pF, RZAP = 330 ohm).

5.2 Thermal Characteristics

Table 5. Thermal Ratings

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
THERMAL RATINGS					
T_A	Ambient Operating Temperature Range	-40	85	°C	
T_J	Operating Junction Temperature Range	-40	125	°C	(5)
T_{ST}	Storage Temperature Range	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	-	Note 7	°C	(6), (7)
8.0 X 8.0 MM, THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\theta JA}$	Junction to Ambient Natural Convection • Single layer board (1s)	-	93	°C/W	(8), (9)
$R_{\theta JMA}$	Junction to Ambient Natural Convection • Four layer board (2s2p)	-	53	°C/W	(8), (10)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Single layer board (1s)	-	80	°C/W	(8), (10)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Four layer board (2s2p)	-	49	°C/W	(8), (10)
$R_{\theta JB}$	Junction to Board	-	34	°C/W	(11)
$R_{\theta JC}$	Junction to Case	-	25	°C/W	(12)
θJT	Junction to Package Top • Natural Convection	-	3.0	°C/W	(13)
13 X 13 MM, THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\theta JA}$	Junction to Ambient Natural Convection • Single layer board (1s)	-	57	°C/W	(8), (9)
$R_{\theta JMA}$	Junction to Ambient Natural Convection • Four layer board (2s2p)	-	36	°C/W	(8), (9), (10)

Table 5. Thermal Ratings *(continued)*

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Single layer board (1s)	-	48	°C/W	(8), (10)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min.) • Four layer board (2s2p)	-	32	°C/W	(8), (10)
$R_{\theta JB}$	Junction to Board	-	22	°C/W	(11)
$R_{\theta JC}$	Junction to Case	-	15	°C/W	(12)
θJT	Junction to Package Top • Natural Convection	-	3.0	°C/W	(13)

Notes

5. Do not operate above 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.
8. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
9. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
10. Per JEDEC JESD51-6 with the board horizontal.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

5.2.1 Power Dissipation

During operation, the temperature of the die should not exceed the maximum junction temperature. To optimize the thermal management scheme and avoid overheating, the MC34708 PMIC provides a thermal management system. The thermal protection is based on a circuit with a voltage output proportional to the absolute temperature.This voltage can be read out via the ADC for specific temperature readouts, see Channel 3 Die Temperature.

The ADEN SPI bit must be set = 1 to enable the comparators for the thermal monitoring (THERM110, THERM120, THERM125, THERM130, and thermal shutdown). With ADEN = 0 the thermal monitors and thermal shutdown are disabled. Interrupts THERM110, THERM120, THERM125, and THERM130 will be generated when respectively crossing in either direction the thresholds specified in Table 6. The temperature range can be determined by reading the THERMxxxS bits.

Thermal protection is integrated to power off the MC34708 PMIC in case of over dissipation. This thermal protection will act above the maximum junction temperature to avoid any unwanted power downs. The protection is debounced for 8.0 ms in order to suppress any (thermal) noise. This protection should be considered as a fail-safe mechanism and therefore the application design should be dimensioned such that this protection is not tripped under normal conditions. The temperature thresholds and the sense bit assignment are listed in Table 6

Table 6. Thermal Protection Thresholds

Parameter	Min	Typ	Max	Units	Notes
Thermal 110 °C threshold (THERM110)	105	110	115	°C	
Thermal 120 °C threshold (THERM120)	115	120	125	°C	
Thermal 125 °C threshold (THERM125)	120	125	130	°C	
Thermal 130 °C threshold (THERM130)	125	130	135	°C	
Thermal warning hysteresis	2.0	-	4.0	°C	(14)
Thermal protection threshold	130	140	150	°C	

Notes
14. Equivalent to approx. 30 mW min, 60 mW max

The THERM1xx thresholds are debounced by the SPI bits DIE_TEMP_DB[1:0], which are programmable from 100 μs to 4.0 ms (4.0 ms by default), see Table 7. When the die temperature crosses these thresholds, the corresponding sense bit will change, and an interrupt will be generated to notify the software the hardware is reaching its thermal limit.

Table 7. Die Temp Debounce Settings

DIE_TEMP_DB [1:0]	Time	Units
00	0.100	ms
01	1.0	ms
10	2.5	ms
11 (default)	4.0	ms

5.3 Electrical Characteristics

5.3.1 Recommended Operating Conditions

Table 8. Recommended Operating Conditions

Symbol	Description (Rating)	Min.	Max.	Unit	Notes
V_{BP}	Main Input Supply	3.0	4.5	V	
V_{LICELL}	LICELL Backup Battery	1.8	3.6	V	
T_A	Ambient Temperature	-40	85	°C	

5.3.2 General PMIC Specifications

Table 9. Pin Logic Thresholds

Pin Name	Internal Termination (19)	Parameter	Load Condition	Min	Max (22)	Unit	Notes
PWRON1, PWRON2, GLBRST	Pull-up	Input Low	47 kOhm	0.0	0.3	V	(16)
		Input High	1.0 MOhm	1.0	VCOREDIG	V	(16)
STANDBY, WDI	Weak Pull-down	Input Low	-	0.0	0.3	V	(21)
		Input High	-	0.9	3.6	V	(21)
CLK32K	CMOS	Output Low	-100 µA	0.0	0.2	V	
		Output High	100 µA	CLK32KVCC - 0.2	CLK32KVCC	V	
CLK32KMCU	CMOS	Output Low	-100 µA	0.0	0.2	V	
		Output High	100 µA	VSRTC - 0.2	VSRTC	V	
RESETB, RESETBMCU, SDWNB, SW1PWGD, SW2PWGD	Open Drain	Output Low	-2.0 mA	0.0	0.4	V	(20)
		Output High	Open Drain	-	3.6	V	(20)
GPIOLV1,2,3,4	CMOS	Input Low	-	0.0	0.3 * GPIOVDD	V	
		Input High	-	0.7 * GPIOVDD	GPIOVDD + 0.3	V	
		Output Low	-	0.0	0.2	V	
		Output High	-	GPIOVDD - 0.2	GPIOVDD	V	
	Open Drain	Output Low	-2.0 mA	0	0.4	V	
		Output High	Open Drain	-	GPIOVDD + 0.3	V	
PWM1, PWM2	CMOS	Output Low	-	0.0	0.2	V	
		Output High	-	GPIOVDD - 0.2	GPIOVDD	V	
CLK, MOSI		Input Low	-	0.0	0.3 * SPIVCC	V	(15)
		Input High	-	0.7 * SPIVCC	SPIVCC + 0.3	V	(15)
CS	Weak Pull-down	Input Low	-	0.0	0.4	V	(15)
		Input High	-	1.1	SPIVCC + 0.3	V	(15)
CS, MOSI (at Booting for SPI / I^2C decoding)	Weak Pull-down on CS	Input Low	-	0.0	0.3 * VCOREDIG	V	(15), (23)
		Input High	-	0.7 * VCOREDIG	VCOREDIG	V	(15), (23)

Table 9. Pin Logic Thresholds

Pin Name	Internal Termination (19)	Parameter	Load Condition	Min	Max (22)	Unit	Notes
MISO, INT	CMOS	Output Low	-100 µA	0.0	0.2	V	MISO (15) (24)
		Output High	100 µA	SPIVCC - 0.2	SPIVCC	V	MISO (15) (24)
PUMS1,2,3,4,5		Input Low PUMSxS = 0	-	0.0	0.3	V	(17)
		Input High PUMSxS = 1	-	1.0	VCOREDIG	V	(17)
ICTEST		Input Low	-	0.0	0.3	V	(18)
		Input High	-	1.1	1.7	V	(18)
SW1CFG, SW4CFG		Input Low	-	0.0	0.3	V	
		Input Mid	-	1.3	2.0	V	
		Input High	-	2.5	3.1	V	

Notes

15. SPIVCC is typically connected to the output of buck regulator SW5 and set to 1.800 V
16. Input has internal pull-up to VCOREDIG equivalent to 200 kOhm
17. Input state is latched in first phase of cold start, refer to Serial Interfaces for a description of the PUMS configuration
18. Input state is not latched
19. A weak pull-down represents a nominal internal pull-down of 100 nA unless otherwise noted
20. RESETB, RESETBMCU, SDWNB, SW1PWGD, SW2PWGD have open drain outputs, external pull-ups are required
21. SPIVCC needs to remain enabled for proper detection of WDI High to avoid involuntary shutdown
22. The maximum should never exceed the maximum rating of the pin as given in Pin Connections
23. The weak pull-down on CS is disabled if a VIH is detected at startup to avoid extra consumption in I^2C mode
24. The output drive strength is programmable

5.3.3 Current Consumption

The current consumption of the individual blocks is described in detail throughout this specification. For convenience, a summary table follows for standard use cases.

Table 10. Current Consumption Summary (27)

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Mode	Description	Typ	Max	Unit	Notes
RTC / Power cut	All blocks disabled, no main battery attached, coin cell is attached to LICELL (at 25 °C only) • RTC Logic • VSRTC • 32 kHz Oscillator • Clk32KMCU buffer active(10 pF load)	4.0	8.0	µA	
OFF (good battery)	All blocks disabled, main battery attached • Digital Core • RTC Logic • VSRTC • 32 kHz Oscillator • CLK32KMCU buffer active (10 pF load)	20	55	µA	
LPM ON Standby	Low Power Mode (Standby pin asserted and ON_STBY_LP=1) • Digital Core • RTC Logic • VCORE Module • VSRTC • CLK32KMCU/CLK32K active (10 pF load) • 32 kHz Oscillator • I_{REF} • SW1, SW2, SW3, SW4A, SW4B, SW5 in PFM (26),(30) • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC in low power mode (25),(28) • Mini-USB	340	424	µA	
ON Standby	• Digital Core • RTC Logic • VCORE module • VSRTC • CLK32KMCU/CLK32K active (10 pF load) • 32 kHz Oscillator • Digital • I_{REF} • SW1, SW2, SW3 SW4A, SW4B, SW5 in PFM (26),(30) • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC on in low power mode (26),(28) • Mini-USB • PLL (for mini USB)	480	561	µA	

Table 10. Current Consumption Summary (27)

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

ON	Typical use case • Digital Core • RTC Logic • VCORE Module • VSRTC CLK32KMCU/CLK32K active (10 pf) • 32 kHz Oscillator • I_{REF} • SW1, SW2, SW3 SW4A, SW4B, SW5 in Apskip SWBST (26),(29),(30) • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC on in low power mode (25),(28) • Digital • PLL • Mini-USB	1600	3000	μA	

Notes
25. Equivalent to approx. 30 mW min, 60 mW max
26. Current in RTC Mode is from LICELL=2.5 V; in all other modes from BP = 3.6 V.
27. External loads are not included (1)
28. VUSB2, VGEN2 external pass PNPs
29. SWBST in auto mode
30. SW4A output 2.5 V

6 General Description

6.1 Features

Power Generation

- Six Buck Switching Regulators
    - Two Single/Dual Phase Buck Regulators
    - Three Single Phase Buck Regulators
    - PFM/Auto Pulse Skip/PWM Operation Mode
    - Dynamic Voltage Scaling
- 5 V Boost Regulator
    - USB On-the-go Support
- Eight LDO Regulators
    - Two with Selectable Internal or External Pass Devices
    - Five with Embedded Pass Devices
    - One with an External PNP Device

Analog to Digital Converter

- Seven General Purpose Channels
- Internal Dedicated Channels
- Resistive Touchscreen Interface

Auxiliary Circuits

- Mini/Micro USB Switch
    - Bidirectional Audio/Data/UART
    - Accessory Identification Circuit
- General Purpose I/Os
- PWM Outputs
- Two general purpose LED Drivers.

Clocking and Oscillators

- Real Time clock
    - Time and day Counters
    - Time of day Alarm
- 32.768 kHz Crystal Oscillator
- Coin Cell Battery Backup and Charger

Serial Interface

- SPI
- I^2C

6.2 Block Diagram

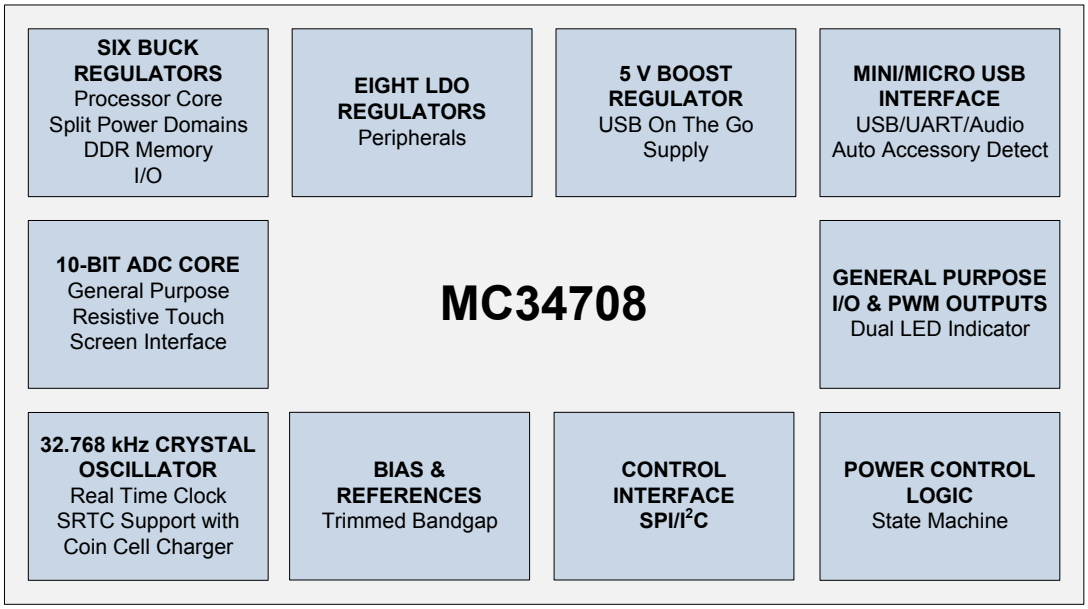


Figure 4. Functional Block Diagram

6.3 Functional Description

The MC34708 Power Management Integrated Circuit (PMIC) represents a complete system power solution in a single package. Designed specifically for use with the Freescale i.MX50/53 families. The MC34708 integrates six multi-mode buck regulators and eight LDO regulators for direct supply of the processor core, memory and peripherals.

The USB switch enables the use of a single, mini or micro USB connector for USB, UART and audio connections, switching the relevant signals to the connector depending on the type of device connected. In addition, the MC34708 also integrates a real time clock, coin cell charger, a 13-channel 10-bit ADC, 5 V USB Boost regulator, two PWM outputs, touch-screen interface, status LED drivers and four GPIOs.

7 Functional Block Description

7.1 Startup Requirements

When power is applied, there is an initial delay of 8.0 ms during which the core circuitry is enabled. The switching and linear regulators are then sequentially enabled in time slot steps of 2.0 ms. This allows the PMIC to limit the inrush current.

The outputs of the switching regulators not enabled are discharged with weak pull-downs on the output to ensure a proper power-up sequence. Any undervoltage detection at BP is masked while the power-up sequencer is running. When the switching regulators are enabled, they will start in PWM mode. After 3.0 ms, the switching regulators will transition to the mode programmed in the SPI register map.

The Power-up mode select pins PUMSx (x = 1, 2, 3, 4, and 5) are used to configure the start-up characteristics of the regulators. Supply enabling and output level options are selected by hardwiring the PUMSx pins. It is recommended to minimize the load during system boot-up by supplying only the essential voltage domains. This allows the start-up transients to be minimized after which the rest of the system power tree can be brought up by software. The PUMSx pins also allow optimization of the supply sequence and default values. Software code can load the required programmable options without any change to hardware.

The state of the PUMSx pins are latched before any of the regulators are enabled, with the exception of VCORE. PUMSx options and start-up configurations are robust to a PCUT event, whether occurring during normal operation or during the 8.0 ms of pre-sequencer initialization, i.e. the system will not end up in an unexpected / undesirable consumption state.

Table 11 shows the initial setup for the voltage level of the switching and linear regulators, and whether they get enabled.

Table 11. Power Up Defaults

i.MX	Reserved	53 LPM	53 DDR2	53 DDR3	53 LVDDR3	53 LVDDR2	50 MDDR	50 LPDDR2	50 LPDDR2	50 MDDR	50 LPDDR2	50 MDDR
PUMS[4:1]	0000-0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
PUMS5=0 VUSB2 VGEN2	Reserved	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP	Ext PNP
PUMS5=1 VUSB2 VGEN2	Reserved	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS	Internal PMOS
SW1A (VDDGP)	Reserved	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
SW1B (VDDGP)	Reserved	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
SW2[31] (VCC)	Reserved	1.225	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2
SW3[31] (VDDA)	Reserved	1.2	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
SW4A[31] (DDR/SYS)	Reserved	1.5	1.8	1.5	1.35	1.2	1.8	1.2	3.15	3.15	3.15	3.15
SW4B[31] (DDR/SYS)	Reserved	1.5	1.8	1.5	1.35	1.2	1.8	1.2	1.2	1.8	1.2	1.8
SW5[31] (I/O)	Reserved	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
SWBST	Reserved	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
VUSB[32]	Reserved	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
VUSB2	Reserved	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5

Table 11. Power Up Defaults

i.MX	Reserved	53 LPM	53 DDR2	53 DDR3	53 LVDDR3	53 LVDDR2	50 MDDR	50 LPDDR2	50 LPDDR2	50 MDDR	50 LPDDR2	50 MDDR
VSRTC	Reserved	1.2	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2
VPLL	Reserved	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
VREFDDR	Reserved	On	On	On	On	On	On	On	On	On	On	On
VDAC	Reserved	2.775	2.775	2.775	2.775	2.775	2.5	2.5	2.5	2.5	2.5	2.5
VGEN1	Reserved	1.2	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2
VGEN2	Reserved	2.5	2.5	2.5	2.5	2.5	3.1	3.1	3.1	3.1	2.5	2.5

Notes

31. The SWx node are activated in APS mode when enabled by the startup sequencer.
32. VUSB regulator is only enabled if 5.0 V is present on VBUS. By default VUSB will be supplied by VBUS. SWBST = 5.0 V powers up as does VUSB, regardless of 5.0 V present on UVBUS. By default VUSB is supplied by SWBST.

The power up sequence is shown in Tables 12 and 13. VCOREDIG, VSRTC, and VCORE, are brought up in the pre-sequencer startup.

Table 12. Power Up Sequence i.MX53

Tap x 2.0 ms	PUMS [4:1] = [0101,0110,0111,1000,1001] (i.MX53)
0	SW2 (VCC)
1	VPLL (NVCC_CKIH = 1.8 V)
2	VGEN2 (VDD_REG= 2.5 V, external PNP
3	SW3 (VDDA)
4	SW1A/B (VDDGP)
5	SW4A/B, VREFDDR (DDR/SYS)
6	
7	SW5 (I/O), VGEN1
8	VUSB [33], VUSB2
9	VDAC

Notes:

33. The VUSB regulator is only enabled if 5.0 V is present on the VBUS pin. By default VUSB will be supplied by the VBUS pin.

Table 13. Power Up Sequence i.MX50

Tap x 2.0 ms	PUMS [4:1] = [0100, 1011, 1100, 1101, 1110, 1111] (i.MX50/I.MX53)
0	SW2
1	SW3
2	SW1A/B
3	VDAC
4	SW4A/B, VREFDDR
5	SW5
6	VGEN2, VUSB2
7	VPLL
8	VGEN1
9	VUSB (34)

Notes:
34. The VUSB regulator is only enabled if 5.0 V is present on the VBUS pin. By default VUSB will be supplied by the VBUS pin.

7.2 Bias and References Block Description and Application Information

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. The bandgap and the rest of the core circuitry is supplied from VCORE. The performance of the regulators is directly dependent on the performance of VCORE and the bandgap. No external DC loading is allowed on VCORE, VCOREDIG, and REFCORE. VCOREDIG is kept powered as long as there is a valid supply and/or coin cell. Table 14 shows the main characteristics of the core circuitry.

Table 14. Core Voltages Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VCOREDIG (DIGITAL CORE SUPPLY)						
$V_{COREDIG}$	Output voltage				V	(35)
	• ON mode	-	1.5	-		
	• OFF mode with good battery and RTC mode	-	1.2	-		
$C_{COREDIG}$	$V_{COREDIG}$ bypass capacitor	-	1.0	-	µF	
VDDLP (DIGITAL CORE SUPPLY - LOWER POWER)						
V_{DDLP}	Output voltage				V	(36)
	• ON mode with good battery	-	1.5	-		
	• OFF mode with good battery	-	1.2	-		
	• RTC mode	-	1.2	-		
C_{DDLP}	V_{DDLP} bypass capacitor	-	100	-	pF	(37)

Table 14. Core Voltages Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VCORE (ANALOG CORE SUPPLY)						
V_{CORE}	Output voltage • ON mode • OFF and RTC mode	 - -	 2.775 0.0	 - -	V	(35)
C_{CORE}	V_{CORE} bypass capacitor	-	1.0	-	µF	
VCOREREF (BANDGAP VOLTAGE/ REGULATOR REFERENCE)						
$V_{COREREF}$	Output voltage	-	1.2	-	V	(35)
	Absolute Accuracy	-	0.5	-	%	
	Temperature Drift	-	0.25	-	%	
$C_{COREREF}$	$V_{COREREF}$ bypass capacitor	-	100	-	nF	

Notes

35. 3.0 V < BP < 4.5 V, no external loading on VCOREDIG, VDDLP, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.
36. Powered by VCOREDIG
37. Maximum capacitance on V_{DDLP} should not exceed 1000 pF, including the board capacitance.

7.3 Clocking and Oscillators

7.3.1 Clock Generation

A system clock is generated for internal digital circuitry as well as for external applications utilizing the clock output pins. A crystal oscillator is used for the 32.768 kHz time base and generation of related derivative clocks. If the crystal oscillator is not running (for example, if the crystal is not present), an internal 32 kHz oscillator will be used instead.

Support is also provided for an external Secure Real Time Clock (SRTC) which may be integrated on a companion system processor IC. For media protection in compliance with Digital Rights Management (DRM) system requirements, the CLK32KMCU can be provided as a reference to the SRTC module where tamper protection is implemented.

7.3.1.1 Clocking Scheme

The internal 32 kHz oscillator is an integrated backup for the crystal oscillator, and provides a 32.768 kHz nominal frequency at ±60% accuracy, if running. The internal oscillator only runs if a valid supply is available at BP, and would not be used as long as the crystal oscillator is active. In absence of a valid supply at the BP supply node, the crystal oscillator will continue to operate as it is powered from the coin cell battery. All control functions will run off the crystal derived frequency, occasionally referred to as “32 kHz” for brevity’s sake.

During the switch-over between the two clock sources (such as when the crystal oscillator is starting up), the output clock is maintained at a stable active low or high phase of the internal 32 kHz clock to avoid any clocking glitches. If the XTAL clock source suddenly disappears during operation, the IC will revert back to the internal clock source. Given the unpredictable nature of the event and the startup times involved, the clock may be absent long enough for the application to shutdown during this transition due to various reasons, for example a sag in the regulator output voltage or absence of a signal on the clock output pins.

A status bit, CLKS, is available to indicate to the processor which clock is currently selected: CLKS = 0 when the internal RC is used and CLKS = 1 if the crystal source is used. The CLKI interrupt bit will be set whenever a change in the clock source occurs, and an interrupt will be generated if the corresponding CLKM mask bit is cleared.

7.3.1.2 Oscillator Specifications

The crystal oscillator has been optimized for use in conjunction with the Micro Crystal CC7V-T1A32.768 kHz-9.0 pF-30 ppm or equivalent (such as Micro Crystal CC5V-T1A or Epson FC135) and is capable of handling its parametric variations. Ensure that the chosen crystal has a typical drive level of 0.5 µW or above to ensure proper operation of the crystal oscillator. Using a crystal with a lower drive level can cause overtone oscillations.

The electrical characteristics of the 32 kHz Crystal oscillator are given in the following table, taking into account the crystal characteristics noted above. The oscillator accuracy depends largely on the temperature characteristics of the crystal. Application circuits can be optimized for required accuracy by adapting the external crystal oscillator network (via component accuracy and/or tuning). Additionally, a clock calibration system is provided to adjust the 32.768 cycle counter that generates the 1.0 Hz timer and RTC registers; see SRTC Support for more detail.

Table 15. Oscillator and Clock Main Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
OSCILLATOR AND CLOCK OUTPUT						
V_{INRTC}	Operating Voltage • Oscillator and RTC Block from BP • Oscillator and RTC Block from LICELL	 1.8 1.8	 - -	 4.5 3.6	V	
I_{INRTC}	Operating Current Crystal Oscillator and RTC Module • All blocks disabled, no main battery attached, coin cell is attached to LICELL	-	2.0	5.0	µA	
$t_{START-RTC}$	RTC oscillator startup time • Upon application of power	-	-	1.0	sec	
V_{RTCLO}	Output Low • CLK32K Output sink 100 µA • CLK32KMCU Output source 50 µA	0.0	-	0.2	V	
V_{RTCHI}	Output High • CLK32K Output source 100 µA • CLK32KMCU Output sink 50 µA	CLK32K VCC -0.2 VSRTC-0.2	- -	CLK32K VCC VSRTC	V	
$t_{CLK32KET}$	CLK32K Rise and Fall Time, CL = 50 pF • CLK32KDRV [1:0] = 00 • CLK32KDRV [1:0] = 01 (default) • CLK32KDRV [1:0] = 10 • CLK32KDRV [1:0] = 11	 - - - -	 6.0 2.5 3.0 2.0	 - - - -	ns	
$t_{CKL32K MCUET}$	CLK32KMCU Rise and Fall Time • CL = 12 pF	-	22	-	ns	
$CLK32K_{DC}$/ $CLK32K MCU_{DC}$	CLK32K and CLK32KMCU Output Duty Cycle • Crystal on XTAL1, XTAL2 pins	45	-	55	%	
	RMS Output Jitter • 1 Sigma for Gaussian distribution	-	-	30	ns RMS	

7.3.2 SRTC Support

When configured for DRM mode (SPI bit DRM = 1), the CLK32KMCU driver will be kept enabled through all operational states to ensure the SRTC module always has its reference clock. If DRM = 0, the CLK32KMCU driver will not be maintained in the Off state.

It is also necessary to provide a means for the processor to do an RTC initiated wake-up of the system if it has been programmed for such capability. This can be accomplished by connecting an open drain NMOS driver to the PWRON pin of the MC34708 PMIC, so it is in effect, a parallel path for the power key. The MC34708 PMIC will not be able to discern the turn on event from a normal power key initiated turn on, but the processor should have the knowledge, since the RTC initiated turn on is generated locally.

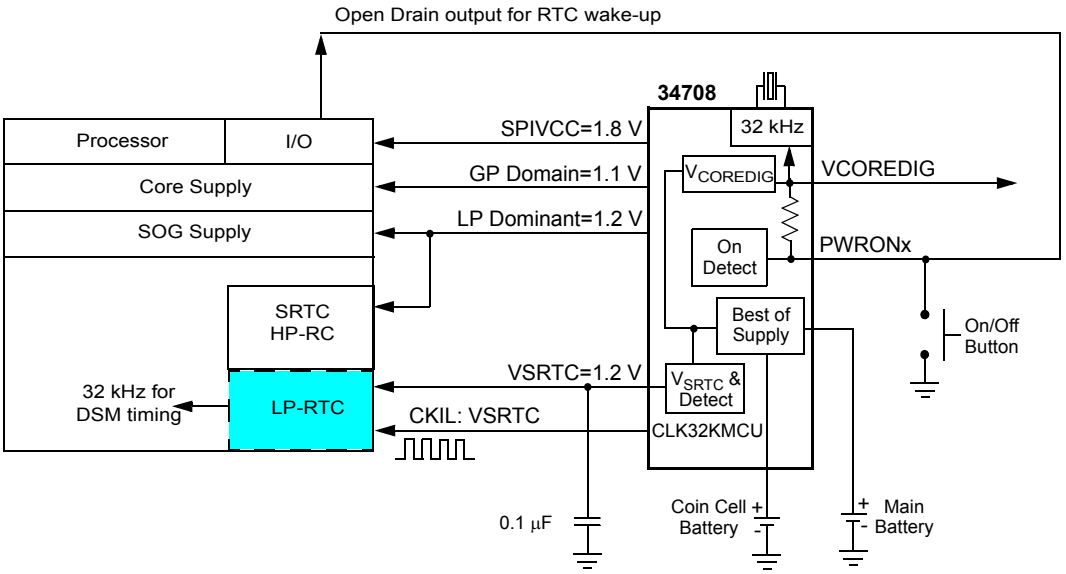


Figure 5. SRTC Block Diagram

7.3.2.1 VSRTC

The VSRTC regulator provides the CLK32KMCU output level. Additionally, it is used to bias the Low Power SRTC domain of the SRTC module integrated on certain FSL processors. The VSRTC regulator is enabled as soon as the RTCPORB is detected. The VSRTC regulator cannot be disabled.

Depending on the configuration of the PUMS[4:0] pins, the VSRTC voltage will be set to 1.3 or 1.2 V. With PUMS[4:0] = (0110, 0111, 1000, or 1001) VSRTC will be set to 1.3 V in ON mode (ON, ON Standby and ON Standby Low Power modes). In OFF and Coin Cell modes the VSRTC voltage will drop to 1.2 V with the PUMS[4:0] = (0110, 0111, 1000, or 1001). With PUMS[4:0] ≠ (0110, 0111, 1000, or 1001), VSRTC will be set to 1.2 V for all modes (ON, ON Standby, LPM ON Standby, OFF, and Coin Cell).

Table 16. VSRTC Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
GENERAL						
V_{SRTCIN}	Operating Input Voltage Range V_{INMIN} to V_{INMAX}				V	
	• Valid Coin Cell range	1.8	-	3.6		
	• Valid BP	1.8	-	4.5		
I_{SRTC}	Operating Current Load Range IL_{MIN} to IL_{MAX}	0.0	-	50	µA	(38)
CO_{SRTC}	Bypass Capacitor Value	-	0.1	-	µF	

Table 16. VSRTC Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VSRTC - ACTIVE MODE - DC						
V_{SRTC}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ • $IL_{MIN} < IL < IL_{MAX}$ • Off and coincell mode	1.15	1.20	1.28	V	
V_{SRTC}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ • $I_{LMIN} < I_L < I_{LMAX}$ • PUMS[4:0] ≠ (0110, 0111, 1000, 1001) • On mode (On, Standby, Standby LPM)	1.15	1.2	1.25	V	
V_{SRTC}	Output Voltage V_{OUT} • VINMIN < V_{IN} < V_{INMAX} • $I_{LMIN} < I_L < I_{LMAX}$ • PUMS[4:0] = (0110, 0111, 1000, 1001) • On mode (On, Standby, Standby LPM)	1.25	1.3	1.35	V	
I_{SRTCQ}	Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0 • VSRTC = 1.2 V • VSRTC = 1.3 V	 - -	 1.7 2.7	 - -	µA	

Notes

38. Valid for BP > 2.4 V and/or LICELL > 2.0 V.

7.3.2.2 Real Time Clock

A Real Time Clock (RTC) is provided with time and day counters as well as an alarm function. The RTC utilizes the 32.768 kHz crystal oscillator for the time base and is powered by the coin cell backup supply when BP has dropped below operational range. In configurations where the SRTC is used, the RTC can be disabled to conserve current drain by setting the RTCDIS bit to a 1 (defaults on at power up).

Time and Day Counters

The 32.768 kHz clock is divided down to a 1.0 Hz time tick which drives a 17 bit Time Of Day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15 bit DAY counter. The DAY counter can count up to 32767 days. The 1.0 Hz time tick can be used to generate a 1HZI interrupt if unmasked.

Time Of Day Alarm

A Time Of Day Alarm (TODA) function can be used to turn on the application and alert the processor. If the application is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. When the TOD counter is equal to the value in TODA and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

Timer Reset

As long as the supply at BP is valid, the real time clock will be supplied from VCOREDIG. If BP is not valid, the real time clock can be backed up from a coin cell via the LICELL pin. When the VSRTC voltage drops to the range of 0.9 - 0.8 V, the RTCPORB reset signal is generated and the contents of the RTC will be reset. Additional registers backed up by coin cell will also reset with RTCPORB. To inform the processor the contents of the RTC are no longer valid due to the reset, a timer reset interrupt function is implemented with the RTCRSTI bit.

RTC Timer Calibration

A clock calibration system is provided to adjust the 32.768 cycle counter that generates the 1.0 Hz timer for RTC timing registers. The general implementation relies on the system processor to measure the 32.768 kHz crystal oscillator against a higher frequency and more accurate system clock such as a TCXO. If the RTC timer needs a correction, a 5-bit 2's complement calibration word can be sent via the SPI to compensate the RTC for inaccuracy in its reference oscillator.

Table 17. RTC Calibration Settings

Code in RTCCAL[4:0]	Correction in Counts per 32768	Relative correction in ppm
01111	+15	+458
00011	+3	+92
00001	+1	+31
00000	0	0
11111	-1	-31
11101	-3	-92
10001	-15	-458
10000	-16	-488

The available correction range should be sufficient to ensure drift accuracy in compliance with standards for DRM time keeping. Note that the 32.768 kHz oscillator is not affected by RTCCAL settings; calibration is only applied to the RTC time base counter. Therefore, the frequency at the clock output CLK32K is not affected.

The RTC system calibration is enabled by programming the RTCCALMODE[1:0] for desired behavior by operational mode.

Table 18. RTC Calibration Enabling

RTCCALMODE	Function
00	RTC Calibration disabled (default)
01	RTC Calibration enabled in all modes except coin cell only
10	Reserved for future use. Do not use.
11	RTC Calibration enabled in all modes

The RTC Calibration circuitry can be automatically disabled when main battery contact is lost or if it is so deeply discharged that the RTC power draw is switched to the coin cell (configured with RTCCALMODE=01).

Because of the low RTC consumption, RTC accuracy can be maintained through long periods of the application being shut down, even after the main battery has discharged. However, the calibration can only be as good as the RTCCAL data provided, so occasional refreshing is recommended to ensure any drift influencing environmental factors have not skewed the clock beyond desired tolerances.

7.3.3 Coin Cell Battery Backup

The LICELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut), the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. This switch over occurs for a BP below 1.8 V threshold with LICELL greater than BP. A small capacitor should be placed from LICELL to ground under all circumstances.

Upon initial insertion of the coin cell, it is not immediately connected to the on chip circuitry. The cell gets connected when the IC powers on, or after enabling the coin cell charger when the IC was already on.

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit. The coin cell voltage is programmable through the VCOIN[2:0] bits. The coin cell charger voltage is programmable in the ON state where the charge current is fixed at ICOINHI.

If COINCHEN=1 when the system goes into Off or User Off state, the coin cell charger will continue to charge to the predefined voltage setting but at a lower maximum current ICOINLO. This compensates for self discharge of the coin cell and ensures if and/or when the main cell gets depleted, the coin cell will be topped off for maximum RTC retention. The coin cell charging will be stopped for the BP below UVDET. The bit COINCHEN itself is only cleared when an RTCPORB occurs.

Table 19. Coin Cell Voltage Specifications

VCOIN[2:0]	Output Voltage
000	2.50
001	2.70
010	2.80
011	2.90
100	3.00
101	3.10
110	3.20
111	3.30

Table 20. Coin Cell Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
COIN CELL CHARGER						
$V_{LICELLACC}$	Voltage Accuracy	-	100	-	mV	
$I_{LICELLON}$	Coin Cell Charge Current in On and Watchdog modes ICOINHI	-	60	-	μA	
$I_{LICELLOFF}$	Coin Cell Charge Current in Off, cold start/warm start, and Low Power Off modes (User Off / Memory Hold) ICOINLO	-	10	-	μA	
$I_{LICELACC}$	Current Accuracy	-	30	-	%	
CO_{LICELL}	LICELL Bypass Capacitor	-	100	-	nF	
	LICELL Bypass Capacitor as coin cell replacement	-	4.7	-	μF	

7.4 Interrupt Management

7.4.1 Control

The system is informed about important events, based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INT pin high; this is true whether the communication interface is configured for SPI or I^2C.

Each interrupt is latched so even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status register, which will also cause the interrupt line to go low. If a new interrupt occurs while the processor clears an existing interrupt bit, the interrupt line will remain high.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the interrupt line will not go high. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the interrupt line will go high after unmasking.

The sense registers contain status and input sense bits, so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Interrupts generated by external events are debounced. Therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary table later in this section. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

7.4.2 Interrupt Bit Summary

Table 21 summarizes all interrupt, mask, and sense bits associated with INT control. For more detailed behavioral descriptions, refer to the related chapters.

Table 21. Interrupt, Mask and Sense Bits

Interrupt	Mask	Sense	Purpose	Trigger	Debounce Time
ADCDONEI	ADCDONEM	-	ADC has finished requested conversions	L2H	0
TSDONEI	TSDONEM	-	Touch screen has finished conversion	L2H	0
TSPENDET	TSPENDETM	-	Touch screen pen detect	Dual	1.0 ms
USBOVP	USBOVPM	USBOVPS	VBUS over-voltage Sense is 1 if above threshold.	Dual	Programmable SUP_OVP_DB
LOWBATT	LOWBATTM	-	Low battery detect Sense is 1 if below LOWBAT threshold	H2L	Programmable VBATTDB
USBDET	USBDETM	USBDETS	USB VBUS detect Sense is 1 if detected	Dual	Programmable VBUSDB
Stuck_Key_RCV	Stuck_Key_RCV_m	-	Stuck key has recovered	L2H	
Stuck_Key	Stuck_Key_m	-	Stuck key detected	L2H	
ADC_Change	ADC_Change_m	ADC_STATUS	ADC result changed Sense is 1 if conversion is completed, 0 if in progress	L2H	
Unknown_Atta	Unknown_Atta_m	-	Unknown accessory detected	L2H	
LKR	LKR_m	-	Remote control long key is released	L2H	
LKP	LKP_m	-	Remote control long key is pressed	L2H	
KP	KP_m	-	Remote control key is pressed	L2H	
Detach	Detach_m	-	Accessory detached	L2H	

Table 21. Interrupt, Mask and Sense Bits

Interrupt	Mask	Sense	Purpose	Trigger	Debounce Time
Attach	Attach_m	-	Accessory attached	L2H	
		ID_GNDS	Sense is 1 if ID pin is grounded		
		ID_FLOATS	Sense is 1 if ID pin is floating		
		ID_DET_ENDS	Sense is 1 if ID resistance detection is complete		
		VBUS_DET_ENDS	Sense is 1 if VBUS PTSI is complete		
SCPI	SCPM	-	Regulator short-circuit protection tripped	L2H	min. 4.0 ms max 8.0 ms
1HZI	1HZM	-	1.0 Hz time tick	L2H	0
TODAI	TODAM	-	Time of day alarm	L2H	0
PWRON1I	PWRON1M	PWRON1S	Power on button 1 event Sense is 1 if PWRON1 is high	H2L	30 ms (39)
				L2H	30 ms
PWRON2I	PWRON2M	PWRON2S	Power on button 2 event Sense is 1 if PWRON2 is high	H2L	30 ms (39)
				L2H	30 ms
SYSRSTI	SYSRSTM	-	System reset through PWRONx pins	L2H	0
WDIRESETI	WDIRESETM	-	WDI silent system restart	L2H	0
PCI	PCM	-	Power cut event	L2H	0
WARMI	WARMM		Warm Start event	L2H	0
MEMHLDI	MEMHLDM		Memory Hold event	L2H	0
CLKI	CLKM	CLKS	32 kHz clock source change Sense is 1 if source is XTAL	Dual	0
RTCRSTI	RTCRSTM	-	RTC reset has occurred	L2H	0
THERM110	THERM110M	THERM110S	Thermal 110C threshold Sense is 1 if above threshold	Dual	Programmable DIE_TEMP_DB
THERM120	THERM120M	THERM120S	Thermal 120C threshold Sense is 1 if above threshold	Dual	Programmable DIE_TEMP_DB
THERM125	THERM125M	THERM125S	Thermal 125C threshold Sense is 1 if above threshold	Dual	Programmable DIE_TEMP_DB
THERM130	THERM130M	THERM130S	Thermal 130C threshold Sense is 1 if above threshold	Dual	Programmable DIE_TEMP_DB
GPIOLVxI	GPIOLVxM	GPIOLVxS	General Purpose input interrupt	Programmable	Programmable

Notes

39. Debounce timing for the falling edge can be extended with PWRONxDBNC[1:0]; refer to Turn On Events for details.

7.5 Power Generation

The MC34708 PMIC provides reference and supply voltages for the application processor as well as peripheral devices.

Six buck (step down) converters and one boost (step up) converter are included. One of the buck regulators can be configured in dual phase, single phase mode, or operate as separate independent outputs (in this case, there are six buck converters). The buck converters provide the supply to processor cores and to other low voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry. The boost converter supplies the VUSB regulator for the USB PHY on the processor. The VUSB regulator is powered from the boost to ensure sufficient headroom for the LDO through the normal discharge range of the main battery.

Linear regulators could be supplied directly from the battery or from one of the switching regulator, and provide supplies for IO and peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. Naming conventions are suggestive of typical or possible use case applications, but the switching and linear regulators may be utilized for other system power requirements within the guidelines of specified capabilities.

Four general purpose I/Os are available. When configured as inputs they can be used as external interrupts.

7.5.1 Power Tree

Refer to the representative tables and text specifying each supply for information on performance metrics and operating ranges.

Table 22 summarizes the available power supplies.

Table 22. Power Tree Summary

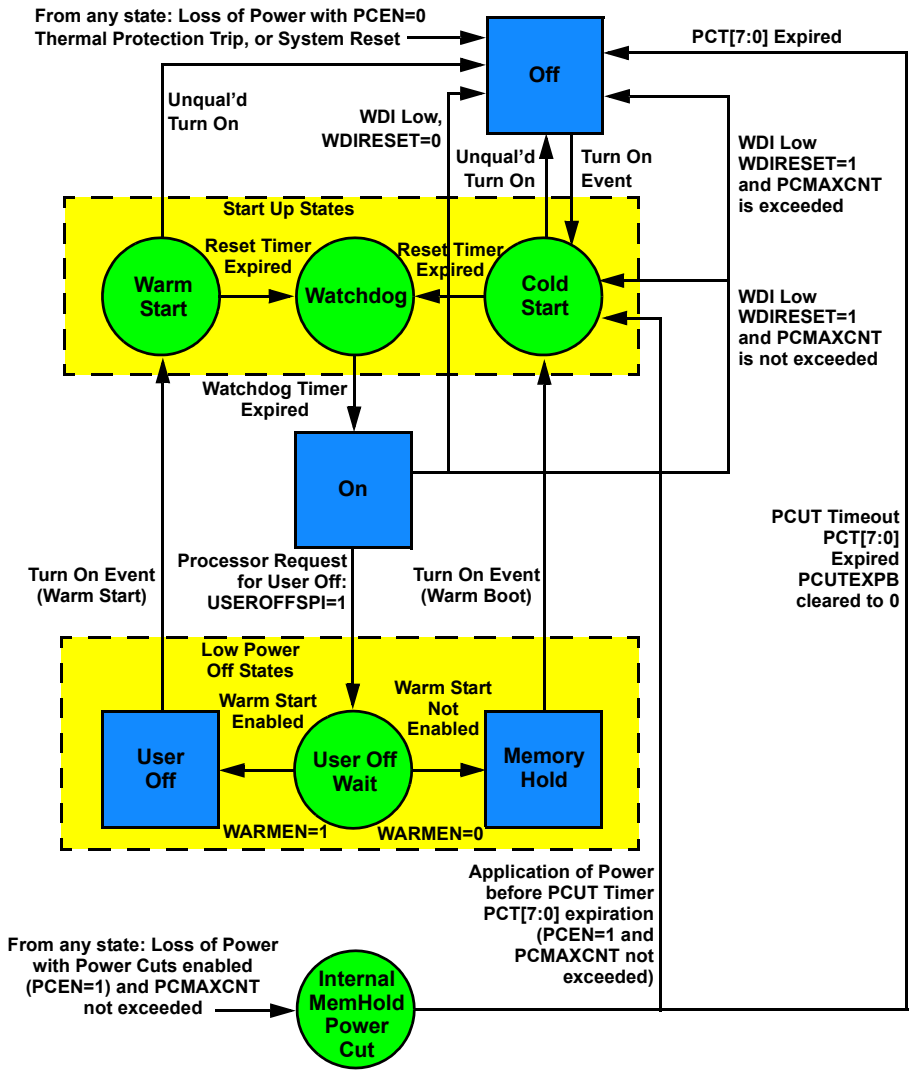
Supply	Purpose (typical application)	Output Voltage (in V)	Load Capability (in mA)
SW1	Buck regulator for processor VDDGP domain	0.650 - 1.4375	2000
SW2	Buck regulator for processor VCC domain	0.650 - 1.4375	1000
SW3	Buck regulator for processor VDD domain and peripherals	0.650 - 1.425	500
SW4A	Buck regulator for DDR memory and peripherals	1.200 – 1.85: 2.5/3.15	500
SW4B	Buck regulator for DDR memory and peripherals	1.200 – 1.85: 2.5/3.15	500
SW5	Buck regulator for I/O domain	1.200 – 1.85	1000
SWBST	Boost regulator for USB OTG	5.00/5.05/5.10/5.15	380
VSRTC	Secure Real Time Clock supply	1.2	0.05
VPLL	Quiet Analog supply	1.2/1.25/1.5/1.8	50
VREFDDR	DDR Ref supply	0.6-0.9	10
VDAC	TV DAC supply, external PNP	2.5/2.6/2.7/2.775	250
VUSB2	VUSB/peripherals supply, internal PMOS	2.5/2.6/2.75/3.0	65
	VUSB/peripherals external PNP	2.5/2.6/2.75/3.0	350
VGEN1	General peripherals supply #1	1.2/1.25/1.3/1.35/1.4/1.45/1.5/1.55	250
VGEN2	General peripherals supply #2, internal PMOS	2.5/2.7/2.8/2.9/3.0/3.1/3.15/3.3	50
	General peripherals supply #2, external PNP	2.5/2.7/2.8/2.9/3.0/3.1/3.15/3.3	250
VUSB	USB Transceiver supply	3.3	100

7.5.2 Modes of Operation

The MC34708 PMIC is fully programmable via the SPI/I^{2}C interface and associated register map. Additional communication is provided by direct logic interfacing, including interrupt, watchdog, and reset. Default startup of the device is selectable by hardwiring the Power Up Mode Select (PUMS) pins.

Power cycling of the application is driven by the MC34708 PMIC. It has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures the supply of the Real Time Clock (RTC), critical internal logic, and other circuits from the coin cell, in case of brief interruptions from the main battery. A charger for the coin cell is included to ensure it is kept topped off until needed.

The MC34708 PMIC provides the timekeeping, based on an integrated low power oscillator running with a standard crystal. This oscillator is used for internal clocking, the control logic, and as a reference for the switcher PLL. The timekeeping includes time of day, calendar, and alarm, and is backed up by coin cell. The clock is driven to the processor for reference and deep sleep mode clocking.



Legend and Notes (refer to text for additional details)
Blue Box = Steady State, no specific timer is running
Green Circle = Transitional State, a specific timer is running, see text
Dashed Boxes = Grouping of States for clarification
WDI has influence only in the "On" state
Complete loss of BP and coin cell power is not represented in the state machine

Figure 6. Power Control State Machine Flow Diagram

The following are text descriptions of the power states of the system for additional details of the state machine to complement the drawing in Figure 6. Note that the SPI control is only possible in the Watchdog, On and User Off Wait states and the interrupt line INT is kept low in all states except for Watchdog and On.

7.5.2.1 Coin Cell

The RTC module is powered from either the battery or the coin cell, due to insufficient voltage at VALWAYS, and the IC is not in a Power Cut. No Turn On event is accepted in the Coin Cell state. Transition out (to the Off state) requires VALWAYS restoration with a threshold above UVDET. RESETB and RESETBMCU are held low in this mode.

The RTC module remains active (32 kHz oscillator + RTC timers), along with VALWAYS level detection to qualify exit to the Off state. VCOREDIG is off and the VDDLP regulator is on, the rest of the system is put into its lowest power configuration.

If the coin cell is depleted (VSTRC drops to 0.9 - 0.8 V while in the Coin Cell state), a complete system reset will occur. At next power application / Turn On event, the system will startup reinitialized with all SPI bits including those that reset on RTCPORB restored to their default states.

7.5.2.2 Off (with good battery)

If the supply VALWAYS is above the UVDET threshold, only the IC core circuitry at VCOREDIG and the RTC module are powered, all other supplies are inactive. To exit the Off state, a valid turn on event is required. No specific timer is running in this state. RESETB, RESETBMCU are held low in this state.

If the supply VALWAYS is below the UVDET threshold, no turn on events are accepted. If a valid coin cell is present, the core gets powered from LICELL. The only active circuitry is the RTC module and the VCORE module powering VCOREDIG at 1.5 V.

7.5.2.3 Cold Start

Cold Start is entered upon a Turn On event from Off, Warm Boot, successful PCUT, or a Silent System Restart. The first 8.0 ms is used for initialization which includes bias generation, PUMSx configuration latching, and qualification of the input supply level BP. The switching and linear regulators are then powered up sequentially to limit the inrush current; see the Power Up section for sequencing and default level details. The reset signals RESETB and RESETBMCU are kept low. The Reset timer starts running when entering Cold Start. The Cold Start state is exited for the Watchdog state and both RESETB and RESETBMCU become high (open drain output with external pull-ups) when the reset timer expires. The input control pins WDI, and STANDBY are ignored.

7.5.2.4 Watchdog

The system is fully powered and under SPI/I^2C control. RESETB and RESETBMCU are high. The Watchdog timer starts running when entering the Watchdog state. When expired, the system transitions to the On state, where WDI will be checked and monitored. The input control pins WDI and STANDBY are ignored while in the Watchdog state.

7.5.2.5 On Mode

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The WDI pin must be high to stay in this state. The WDI IO supply voltage is referenced to SPIVCC (normally connected to SW5 = 1.8 V); SPIVCC must therefore remain enabled to allow for proper WDI detection. If WDI goes low, the system will transition to the Off state or Cold Start (depending on the configuration; refer to the section on Silent System Restart with WDI Event for details).

7.5.2.6 User Off Wait

The system is fully powered and under SPI control. The WDI pin no longer has control over the part. The Wait mode is entered by a processor request for user off by setting the USEROFFSPI bit high. This is normally initiated by the end user via the power key; upon receiving the corresponding interrupt, the system will determine if the product has been configured for User Off or Memory Hold states (both of which first require passing through User Off Wait) or just transition to Off.

The Wait timer starts running when entering User Off Wait state. This leaves the processor time to suspend or terminate its tasks. When expired, the Wait state is exited for User Off state or Memory Hold state depending on warm starts being enabled or not via the WARMEN bit. The USEROFFSPI bit is being reset at this point by RESETB going low.

7.5.2.7 Memory Hold and User Off (Low Power Off States)

As noted in the User Off Wait description, the system is directed into low power Off states based on a SPI command in response to an intentional turn off by the user. The only exit then will be a turn on event. To the user, the Memory Hold and User Off states look like the product has been shut down completely. However, a faster startup is facilitated by maintaining external memory in self-refresh state (Memory Hold and User Off state) as well as powering portions of the processor core for state retention (User Off only). The Switching regulator mode control bits allow selective powering of the buck regulators for optimizing the supply behavior in the low power Off states. Linear regulators and most functional blocks are disabled (the RTC module, SPI bits resetting with RTCPORB, and Turn On event detection are maintained).

By way of example, the following descriptions assume the typical use case where SW1 supplies the processor core(s), SW2 is applied to the processor's VCC domain, SW3 supplies the processor's internal memory/peripherals, and SW4 supplies the external memory, and SW5 supplies the I/O rail. The buck regulators are intended for direct connection to the aforementioned loads.

7.5.2.8 Memory Hold

RESETB and RESETBMCU are low, and both CLK32K and CLK32KMCU are disabled (CLK32KMCU active if DRM is set). To ensure that SW1, SW2, SW3, and SW5 shut off in Memory Hold, appropriate mode settings should be used such as SW1MHMODE, = SW2MHMODE, = SW3MHMODE, = SW5MHMODE set to = 0 (refer to the mode control description later in this section). Since SW4 should be powered in PFM mode, SW4MHMODE could be set to 1.

Upon a Turn On event, the Cold Start state is entered, the default power up values are loaded, and the MEMHLDI interrupt bit is set. A Cold Start out of the Memory Hold state will result in shorter boot times compared to starting out of the Off state, since software does not have to be loaded and expanded from flash. The startup out of Memory Hold is also referred to as Warm Boot. No specific timer is running in this state.

Buck regulators configured to stay on in MEMHOLD mode by their SWxMHMODE settings will not be turned off when coming out of MEMHOLD and entering a Warm Boot. The switching regulators will be reconfigured for their default settings as selected by the PUMSx pins in the normal time slot affecting them.

7.5.2.9 User Off

RESETB is low and RESETBMCU is kept high. The 32 kHz peripheral clock driver CLK32K is disabled; CLK32KMCU (connected to the processor's CKIL input) is maintained in this mode if the CLK32KMCUEN and USEROFFCLK bits are both set, or if DRM is set.

The memory domain is held up by setting SW4UOMODE = 1. Similarly, the SW1 and/or SW2 and/or SW3 supply domains can be configured for SWxUOMODE=1 to keep them powered through the User Off event. If one of the switching regulators can be shut down in User Off, its mode bits would typically be set to 0.

Since power is maintained for the core (which is put into its lowest power state), and since MCU RESETBMCU does not trip, the processor's state may be quickly recovered when exiting USEROFF upon a turn on event. The CLK32KMCU clock can be used for very low frequency / low power idling of the core(s), minimizing battery drain, while allowing a rapid recovery from where the system left off before the USEROFF command.

Upon a Turn On event, Warm Start state is entered, and the default power up values are loaded. A Warm Start out of User Off will result in an almost instantaneous startup of the system, since the internal states of the processor were preserved along with external memory. No specific timer is running in this mode.

7.5.2.10 Warm Start

Entered upon a Turn On event from User Off. The first 8.0 ms is used for initialization, which includes bias generation, PUMSx latching, and qualification of the input supply level BP. The switching and linear regulators are then powered up sequentially to limit the inrush current; see Startup Requirements for sequencing and default level details. If SW1, SW2, SW3, SW4, and/or SW5, were configured to stay on in User Off mode by their SWxUOMODE settings, they will not be turned off when coming out of User Off and entering a Warm Start. The buck regulators will be reconfigured for their default settings as selected by the PUMSx pins in the respective time slot defined in the sequencer selection.

RESETB is kept low and RESETBMCU is kept high. CLK32KMCU is kept active if CLK32KMCU was set. The reset timer starts running when entering Warm Start. When expired, the Warm Start state is exited for the Watchdog state, a WARMI interrupt is generated, and RESETB will go high.

7.5.2.11 Internal MemHold Power Cut

As described in the Power Cut Description, a momentary power interruption will put the system into the Internal MemHold Power Cut state if PCUTs are enabled. The backup coin cell will now supply the MC34708 core, along with the 32 kHz crystal oscillator, the RTC system, and coin cell backed up registers. All regulators will be shut down to preserve the coin cell and RTC as long as possible.

Both RESETB and RESETBMCU are tripped, bringing the entire system down, along with the supplies and external clock drivers, so the only recovery out of a Power Cut state is to reestablish power and initiate a Cold Start.

If the PCT timer expires before power is re-established, the system transitions to the Off state and awaits a sufficient supply recovery.

7.5.3 Power Control Logic

7.5.3.1 Power Cut Description

When the supply at VALWAYS drops below the UVDET threshold, due to battery bounce or battery removal, the Internal MemHold Power Cut state is entered and a Power Cut (PCUT) timer starts running. The backup coin cell will now supply the RTC as well as the on chip memory registers and some other power control related bits. All other supplies will be disabled.

The maximum duration of a power cut is determined by the PCUT timer PCT [7:0] preset via the SPI. When a PCUT occurs, the PCUT timer will be started. The contents of PCT [7:0] does not reflect the actual count down value, but will keep the programmed value, and therefore does not have to be reprogrammed after each power cut.

If power is not re-established above the LOWBATT threshold before the PCUT timer expires, the state machine transitions to the Off mode at expiration of the counter, and clears the PCUTEXB bit by setting it to 0. This transition is referred to as an “unsuccessful” PCUT. In addition the PMIC will bring the SDWNB pin low for one 32 kHz clock cycle before powering down.

Upon re-application of power before expiration (a “successful PCUT”, defined as VALWAYS first rising above the UVDET threshold and then battery above the LOWBATT threshold before the PCUT timer expires), a Cold Start is engaged after the UVTIMER has expired.

In order to distinguish a non-PCUT initiated Cold Start from a Cold Start after a PCUT, the PCI interrupt should be checked by software. The PCI interrupt is cleared by software or when cycling through the Off state.

Because the PCUT system quickly disables the entire power tree, the battery voltage may recover to a level with the appearance of a valid supply once the battery is unloaded. However, upon a restart of the IC and power sequencer, the surge of current through the battery and trace impedances can once again cause the BP node to droop below UVDET. This chain of cyclic power down / power up sequences is referred to as “ambulance mode”, and the power control system includes strategies to minimize the chance of a product falling into and getting stuck in ambulance mode.

First, the successful recovery out of a PCUT requires the VABTT node to rise above LOBATT threshold, providing hysteretic margin from the LOBATTT (H to L) threshold. Second, the number of times the PCUT mode is entered is counted with the counter PCCOUNT [3:0], and the allowed count is limited to PCMAXCNT [3:0] set through SPI. When the contents of both become equal, then the next PCUT will not be supported and the system will go to Off mode, after the PCUT time expires.

After a successful power up after a PCUT (i.e., valid power is reestablished, the system comes out of reset, and the processor reassumes control), software should clear the PCCOUNT [3:0] counter. Counting of PCUT events is enabled via the PCCOUNTEN bit. This mode is only supported if the power cut mode feature is enabled by setting the PCEN bit. When not enabled, then in case of a power failure, the state machine will transition to the Off state. SPI control is not possible during a PCUT event and the interrupt line is kept low. SPI configuration for PCUT support should also include setting the PCUTEXPB = 1 (See Silent Restart from PCUT Event).

7.5.3.2 Silent Restart from PCUT Event

If a short duration power cut event occurs (such as from a battery bounce, for example), it may be desirable to perform a silent restart, so the system is reinitialized without alerting the user. This can be facilitated by setting the PCUTEXPB bit to “1” at booting or after a Cold Start. This bit resets on RTCPORB, therefore any subsequent Cold Start can first check the status of PCUTEXPB and the PCI bit. The PCUTEXPB is cleared to “0” when transitioning from PCUT to Off. If there was a PCUT interrupt and PCUTEXPB is still “1”, then the state machine has not transitioned through Off, which confirms the PCT timer has not expired during the PCUT event (i.e., a successful power cut). In this case, a silent restart may be appropriate.

If PCUTEXPB is found to be “0” after the Cold Start where PCI is found to be “1”, then it is inferred the PCT timer has expired before power was re-established. This indicates an unsuccessful power cut or first power up, so the startup user greeting may be desirable for playback.

7.5.3.3 Silent System Restart with WDI Event

A mechanism is provided for recovery if the system software somehow gets into an abnormal state which requires a system reset, but it is desired to make the reset a silent event so as to happen without user awareness. The default response to WDI going low is for the state machine to transition to the Off state (when WDIRESET = 0). However, if WDIRESET = 1, the state machine will go to Cold Start without passing through Off mode (i.e., does not generate an OFFB signal).

A WDIRESET event will generate a maskable WDIRESETI interrupt and also increment the PCCOUNT counter. This function is unrelated to PCUTs, but it shares the PCUT counter so the number of silent system restarts can be limited by the programmable PCMAXCNT counter.

When PCUT support is used, the software should set the PCUTEXPB bit to “1”. Since this bit resets with RTCPORB, it will not be reset to “0” if a WDI falls and the state machine goes straight to the Cold Start state. Therefore, upon a restart, software can discern a silent system restart if there is a WDIRESETI interrupt and PCUTEXPB = 1. The application may then determine an inconspicuous restart without fanfare may be more appropriate than launching into the welcoming routine.

A PCUT event does not trip the WDIRESETI bit.

Note that the system response to WDI is gated by the Watchdog timer—once the timer has expired, the system will respond as programmed by WDIRESET as described above.

Applications should make sure there is time for switching regulator outputs to discharge before re-asserting WDI.

7.5.3.4 Turn On Events

When in Off mode, the circuit can be powered on via a Turn On event. The Turn On events are listed by the following. To indicate to the processor what event caused the system to power on, an interrupt bit is associated with each of the Turn On events. Masking the interrupts related to the turn on events will not prevent the part to turn on except for the time of day alarm. If the part was already on at the time of the turn on event, the interrupt is still generated.

- **Power Button Press:** PWRON1 or PWRON2 pulled low with corresponding interrupts and sense bits PWRON1I, or PWRON2I and PWRON1S, or PWRON2S. A power on/off button is connected from PWRONx to ground. The PWRONx can be hardware debounced through a programmable debouncer PWRONxDBNC [1:0] to avoid a response upon a very short (i.e., unintentional) key press. BP should be above UVDET to allow a power up. The PWRONxI interrupt is generated for both the falling and the rising edge of the PWRONx pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONxDBNC[1:0] as defined in the following table. The PWRONxI interrupt is cleared by software or when cycling through the Off mode.

Table 23. PWRONx Hardware Debounce Bit Settings[40]

Bits	State	Turn On Debounce (ms)	Falling Edge INT Debounce (ms)	Rising Edge INT Debounce (ms)
PWRONxDBNC[1:0]	00	0.0	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

Notes
40. The sense bit PWRONxS is not debounced and follows the state of the PWRONx pin.

- **Battery Attach:** This occurs when BP crosses the LOWBATT threshold which is equivalent to attaching a charged battery to the product.
- **USB Attach:** VBUS pulled high with corresponding interrupt and sense bits USBDET and USBDETS. This is equivalent to plugging in a USB cable connected to a host powering the VBUS line. The battery voltage should be above LOWBATT. For details on the USB detection, see Mini/Micro USB Switch.
- **RTC Alarm:** TOD and DAY become equal to the alarm setting programmed. This allows powering up a product at a preset time. BP should be above LOWBATT. For details and related interrupts, see Real Time Clock.
- **System Restart:** System restart which may occur after a system reset as described earlier in this section. This is an optional function, see Turn Off Events. BP should be above LOWBATT.
- **Global System Reset:** The global reset feature powers down the part, resets the SPI registers to their default value including all the RTCPORB registers (except the DRM bit, and the RTC registers), and then powers back on. To enable a global reset, the GLBRST pin needs to be pulled low for greater than GLBRSTTMR [1:0] seconds and then pulled back high (defaults to 12 s). BP should be above LOWBATT.

Table 24. Global Reset Time Settings

Bits	State	Time (s)
GLBRSTTMR[1:0]	00	INVALID
	01	4
	10	8
	11 (default)	12

7.5.3.5 Turn Off Events

- **Power Button Press (via WDI):** User shutdown of a product is typically done by pressing the power button connected to the PWRONx pin. This will generate an interrupt (PWRONxI), but will not directly power off the part. The product is powered off by the processor's response to this interrupt, which will be to pull WDI low. Pressing the power button is therefore, under normal circumstances, not considered as a turn off event for the state machine. However, since the button press power down is the most common turn off method for end products, it is described in this section as the product implementation for a WDI initiated Turn Off event. Note that the software can configure a user initiated power down, via a power button press for transition to a Low Power Off mode (Memory Hold or User Off) for a quicker restart than the default transition into the Off state.
- **Power Button System Reset:** A secondary application of the PWRONx pins is the option to generate a system reset. This is recognized as a Turn Off event. By default, the system reset function is disabled but can be enabled by setting the PWRONxRSTEN bits. When enabled, a four second long press on the power button will cause the device to go to the Off mode, and as a result, the entire application will power down. An interrupt SYSRSTI is generated upon the next power up. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.
- **Thermal Protection:** If the die gets overheated, the thermal protection will power off the part to avoid damage. A Turn On event will not be accepted while the thermal protection is still being tripped. The part will remain in Off mode until cooling sufficiently to accept a Turn On event. There are no specific interrupts related to this, other than the warning interrupts.
- **BP lower than VBAT_TRKL:** When the voltage at BP drops below VBAT_TRKL[1:0] - 100mV, the state machine will transition to the Off mode. The SDWNB pin is used to notify the processor that the PMIC is going to immediately shutdown. The PMIC will bring the SDWNB pin low for one 32 kHz clock cycle before powering down. This signal will then be brought back high into the power off state.

Table 25. Turn OFF Voltage Threshold

VBAT_TRKL[1:0]	Turn off Voltage threshold
00	2.8
01	2.9
10	3.0 (default)
11	3.1

7.5.3.6 Timers

The different timers as used by the state machine are listed in Table 26. This listing does not include RTC timers for timekeeping. A synchronization error of up to one clock period may occur with respect to the occurrence of an asynchronous event, the duration listed below is therefore the effective minimum time period.

Table 26. Timer Main Characteristics

Timer	Duration	Clock
Under-voltage Timer	4.0 ms	32 k/32
Reset Timer	40 ms	32 k/32
Watchdog Timer	128 ms	32 k/32
Power Cut Timer	Programmable 0 to 8 seconds in 31.25 ms steps	32 k/1024

7.5.3.6.1 Timing Diagrams

A Turn On event timing diagrams shown in Figure 7.

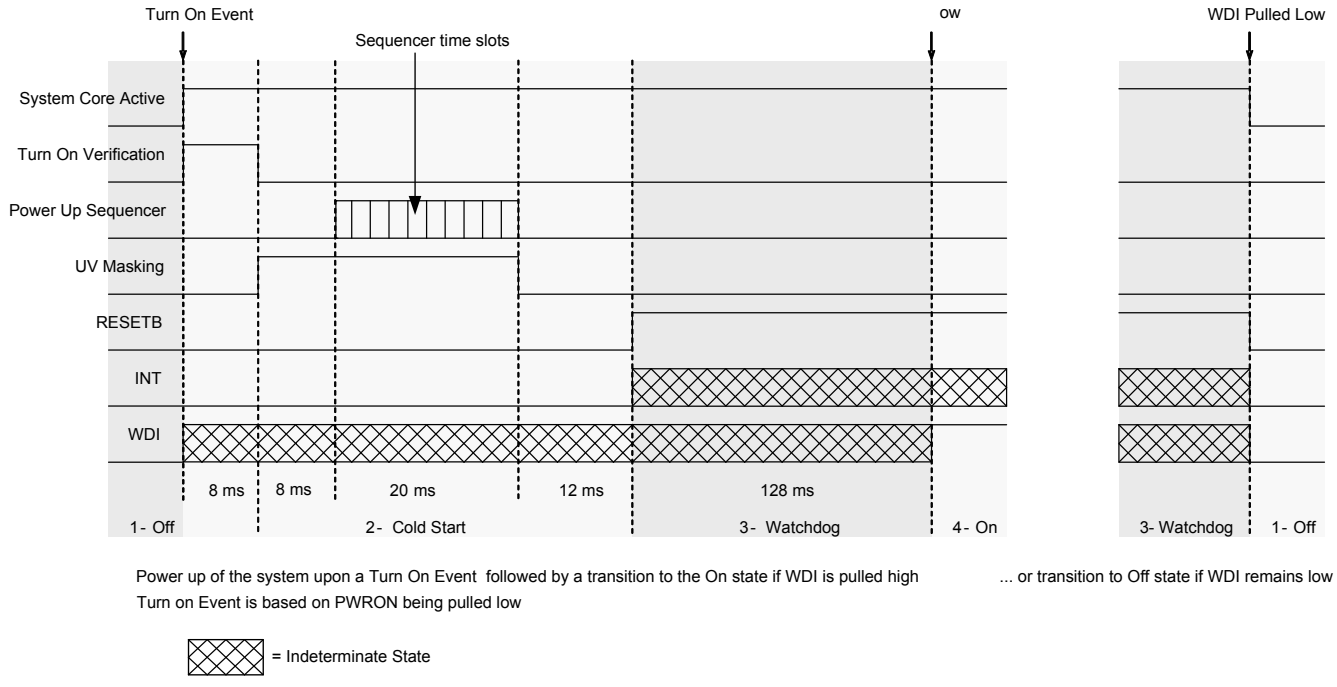


Figure 7. Power Up Timing Diagram

7.5.3.7 Power Monitoring

The voltage at BATT and BP are monitored by detectors as summarized in Table 27.

Table 27. LOWBATT Detection Thresholds

		Threshold in V		
Bit setting[41]		UVDET (V)	L to H transition (Power on)[42],[43]	H to L transition (Low battery detect)[42],[43]
LOWBATT1	LOWBATT0		LOWBATT	LOWBATT
0	0	3.1 (Rising) 2.65 (Falling)	3.1	3.0
0	1	3.1 (Rising) 2.65 (Falling)	3.2	3.1
1	0	3.1 (Rising) 2.65 (Falling)	3.3	3.2
1	1	3.1 (Rising) 2.65 (Falling)	3.4	3.3

Notes
41. Default setting for LOWBATT[1:0] is 11.
42. The above specified thresholds are ±50 mV accurate for the indicated transition
43. A hysteresis is applied to the detectors on the order of 100 mV

The UVDET and LOWBATT thresholds are related to the power on/off events as described earlier in this chapter. The LOWBATT threshold when transitioned from low to a high is used to power on the MC34708. The LOWBATT threshold when transitioned from high to low, is used as a low battery detect warning. An interrupt LOWBAT is generated when dropping below the high to low threshold to indicate to the processor the battery is weak and a shutdown is imminent.

The LOWBATT detection threshold is debounced by the VBATTDB[2:0] SPI bits shown in Table 28.

Table 28. VBATTDB Debounce Times

VATTDB[1:0]	Debounce Time
00	0 (default)
01	2 RTC clock cycles
10	4 RTC clock cycles
11	8 RTC clock cycles

7.5.3.8 Power Saving

7.5.3.8.1 System Standby

A product may be designed to go into DSM (Deep Sleep Mode) after periods of inactivity, the STANDBY pin is provided for board level control of timing in and out of such deep sleep modes.

When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the switching regulators or disabling some regulators. This can be obtained by controlling the STANDBY pin. The configuration of the regulators in standby is pre-programmed through the SPI.

A lower power standby mode can be obtained by setting the ON_STBY_LP SPI bit to a one. With the ON_STBY_LP SPI bit set and the STANDBY pin asserted a lower power standby will be entered. In the on Standby Low Power mode, the switching Regulators should all be programmed into PFM mode and the LDO's should be configured to Low Power mode when the STANDBY pin is asserted. The PLL is disabled in this mode so the mini USB will not be able to detect if an audio device, UART, or a USB OTG device is attached. It will require the software to wake up occasionally to allow the mini-USB to detect if a device

is attached by de-asserting the STANDBY pin and waking up for a period to see if a device is attached and then re-asserting Standby if a device has not been detected. If a device has been detected then the software can bring up the appropriate application etc.

Note the STANDBY pin is programmable for Active High or Active Low polarity, and decoding of a Standby event will take into account the programmed input polarity associated with each pin. For simplicity, Standby will generally be referred to as active high throughout this document, but as defined in Table 29, active low operation can be accommodated. Finally, since STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes.

Table 29. Standby Pin and Polarity Control

STANDBY (Pin)	STANDBYINV (SPI bit)	STANDBY Control[44]
0	0	0
0	1	1
1	0	1
1	1	0

Notes
44. STANDBY = 0: System is not in Standby STANDBY = 1: System is in Standby

The state of the STANDBY pin only has influence in On mode, and are therefore it is ignored during start up and in the Watchdog phase. This allows the system to power up without concern of the required Standby polarities since software can make adjustments accordingly as soon as it is running.

A command to transition to one of the low power Off states (User Off or Memory Hold, initiated with USE-ROFFSPI=1) redefines the power tree configuration based on SWxMODE programming, and has priority over Standby (which also influences the power tree configuration).

7.5.3.8.2 Standby Delay

A provision to delay the Standby response is included. This allows the processor and peripherals, some time after a Standby instruction has been received, to terminate processes to facilitate seamless Standby exiting and re-entrance into Normal operating mode.

A programmable delay is provided to hold off the system response to a Standby event. When enabled (STBYDLY = 01, 10, or 11), STBYDLY will delay the STANDBY initiated response for the entire IC until the STBYDLY counter expires.

Note that this delay is applied only when going into Standby, and no delay is applied when coming out of Standby. Also, an allowance should be accounted for synchronization of the asynchronous Standby event and the internal clocking edges (up to a full 32 kHz cycle of additional delay).

Table 30. Delay of STANDBY- Initiated Response

STBYDLY[1:0]	Function
00	No Delay
01	One 32 k period (default)
10	Two 32 k periods
11	Three 32 k periods

7.5.4 Buck Switching Regulators

Six buck switching regulators are provided with integrated power switches and synchronous rectification. In a typical application, SW1 and SW2 are used for supplying the application processor core power domains. Split power domains allow independent DVS control for processor power optimization, or to support technologies with a mix of device types with different voltage ratings. SW3 is used for powering internal processor memory as well as low voltage peripheral devices and interfaces which can run at the same voltage level. SW4A/B is used for powering external DDR memory as well as low voltage peripheral devices and interfaces, which can run at the same voltage level. SW5 is used to supply the I/O domain for the system.

The buck regulators are supplied from the system supply BP, which is drawn from the main battery or the external battery charger (when present).

The switching regulators can operate in different modes depending on the load conditions. These modes can be set through the SPI/I^2C and include a PFM mode, an Automatic Pulse Skipping mode (APS), and a PWM mode. The previous selection is optimized to maximum battery life based on load conditions.

Table 31. Buck Operating Modes

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged
PFM	The regulator is switched on and set to PFM mode operation. In this mode, the regulator is always running in PFM mode. Useful at light loads for optimized efficiency.
APS	The regulator is switched on and set to Automatic Pulse Skipping. In this mode the regulator moves automatically between pulse skipping and full PWM mode depending on load conditions.
PWM	The regulator is switched on and set to PWM mode. In this mode the regulator is always in full PWM mode operation regardless of load conditions.

Buck modes of operation are programmable for explicitly defined or load-dependent control.

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms (typical) after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes. The regulators are turned on in APS mode by default. After the start-up sequence is complete, all switching regulators should be set to PFM/PWM mode, depending on system load for best performance.

Point of load feedback is intended for minimizing errors due to board level IR drops.

7.5.4.1 General Control

Operational modes of the Buck regulators can be controlled by direct SPI programming, altered by the state of the STANDBY pin, by direct state machine influence (entering Off or low power Off states, for example), or by load current magnitude when so configured (APS mode). Available modes include PWM, PFM, APS and OFF. For light loading, the regulators should be put into PFM mode to optimize efficiency.

Provisions are made for maintaining PFM operation in User off and Memhold modes, to support state retention for faster startup from the Low Power Off modes for Warm Start or Warm Boot. SWxMODE[3:0] bits will be reset to their default values defined by PUMSx settings by the startup sequencer.

Table 32 summarizes the Buck regulators programmability for Normal and Standby modes.

Table 32. Switching regulator Mode Control for Normal and Standby Operation

SWxMODE[3:0]	Normal Mode	Standby Mode
0000	Off	Off
0001	PWM	Off
0010	Reserved	Reserved
0011	PFM	Off

Table 32. Switching regulator Mode Control for Normal and Standby Operation

SWxMODE[3:0]	Normal Mode	Standby Mode
0100	APS	Off
0101	PWM	PWM
0110	PWM	APS
0111	Off	Off
1000	APS	APS
1001	Reserved	Reserved
1010	Reserved	Reserved
1011	Reserved	Reserved
1100	APS	PFM
1101	PWM	PFM
1110	Reserved	Reserved
1111	PFM	PFM

In addition to controlling the operating mode in Standby, the voltage setting can be changed. The transition in voltage is handled in a controlled slope manner, see Dynamic Voltage Scaling for details. Each regulator has an associated set of SPI bits for Standby mode set points. By default, the Standby settings are identical to the non-standby settings which are initially defined by PUMSx programming.

The actual operating mode of the Switching regulators as a function of the STANDBY pin is not reflected through the SPI. In other words, the SPI will read back what is programmed in SWxMODE[3:0], not the actual state that may be altered as described previously.

Two tables follow for mode control in the low power Off states. Note that a low power Off activated SWx should use the Standby set point as programmed by SWxSTBY[4:0]. The activated regulator(s) will maintain settings for mode and voltage until the next startup event. When the respective time slot of the startup sequencer is reached for a given regulator, its mode and voltage settings will be updated the same as if starting out of the Off state (except switching regulators active through a low power Off mode will not be off when the startup sequencer is started).

Table 33. Switching regulator Control In Memory Hold

SWxMHMODE	Memory Hold Operational Mode (45)
0	Off
1	PFM

Notes:

45. For Memory Hold mode, an activated SWx should use the Standby set point as programmed by SWxSTBY[4:0].

Table 34. Switching regulator Control In User Off

SWxUOMODE	User Off Operational Mode (46)
0	Off
1	PFM

Notes:

46. For User Off mode, an activated SWx should use the Standby set point as programmed by SWxSTBY[4:0].

In normal steady state operating mode, the SWxPWGD pin is high. When the SWx set point is changed to a higher or lower set point, the SWxPWGD pin will go low and will go high again when the higher/lower set point is reached.

7.5.4.2 Switching Frequency

A PLL generates the switching system clocking from the 32.768 kHz crystal oscillator reference. The switching frequency can be programmed to 2.0 MHz or 4.0 MHz by setting the PLLX SPI bit as shown in Table 35.

Table 35. Buck Regulator Frequency

PLLX	Switching Frequency (Hz)
0	2 000 000
1	4 000 000

The clocking system provides a near instantaneous activation when the Switching regulators are enabled or when exiting PFM operation for PWM mode. The PLL can be configured for continuous operation with PLLEN = 1.

7.5.4.3 SW1

SW1 is fully integrated synchronous Buck PWM voltage mode control DC/DC regulator. It can be operated in single phase/dual phase mode. The operating mode of the switching regulators is configured by the SW1CFG pin. The SW1CFG pin is sampled at startup.

Table 36. SW1 Configuration

SW1CFG	SW1A/B Configuration Mode
VCOREDIG	Single Phase Mode
Ground	Dual Phase Mode

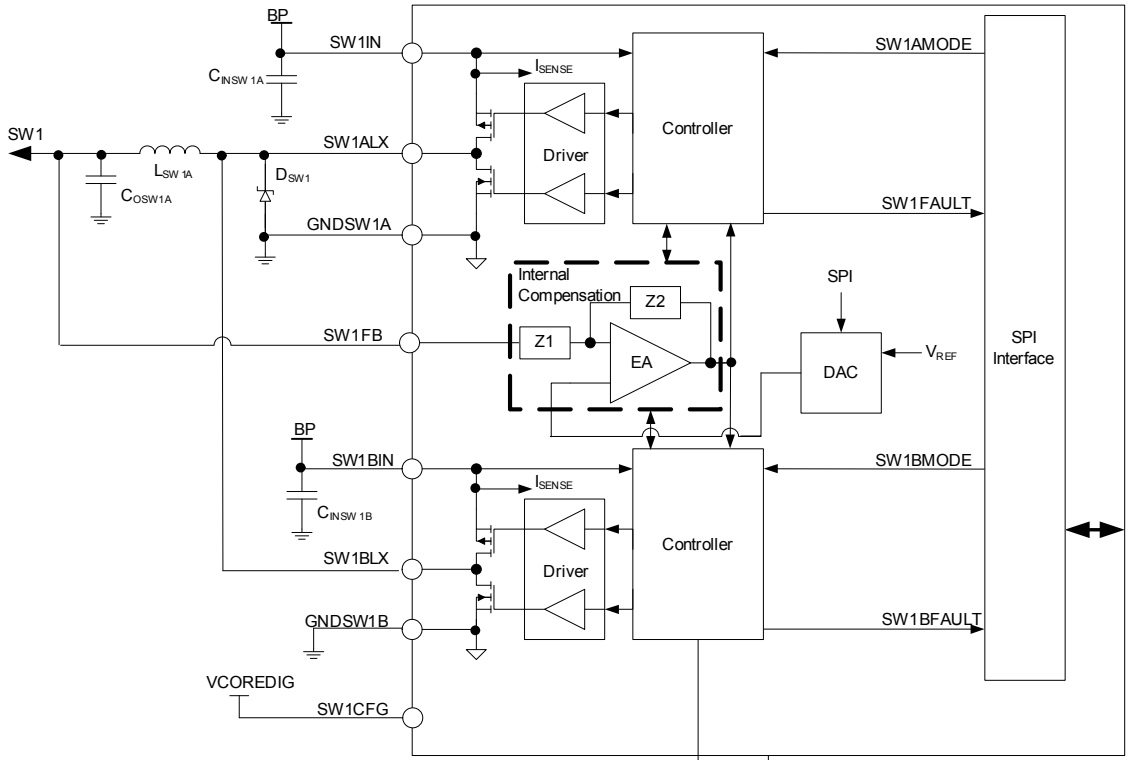


Figure 8. SW1 Single Phase Output Mode Block Diagram

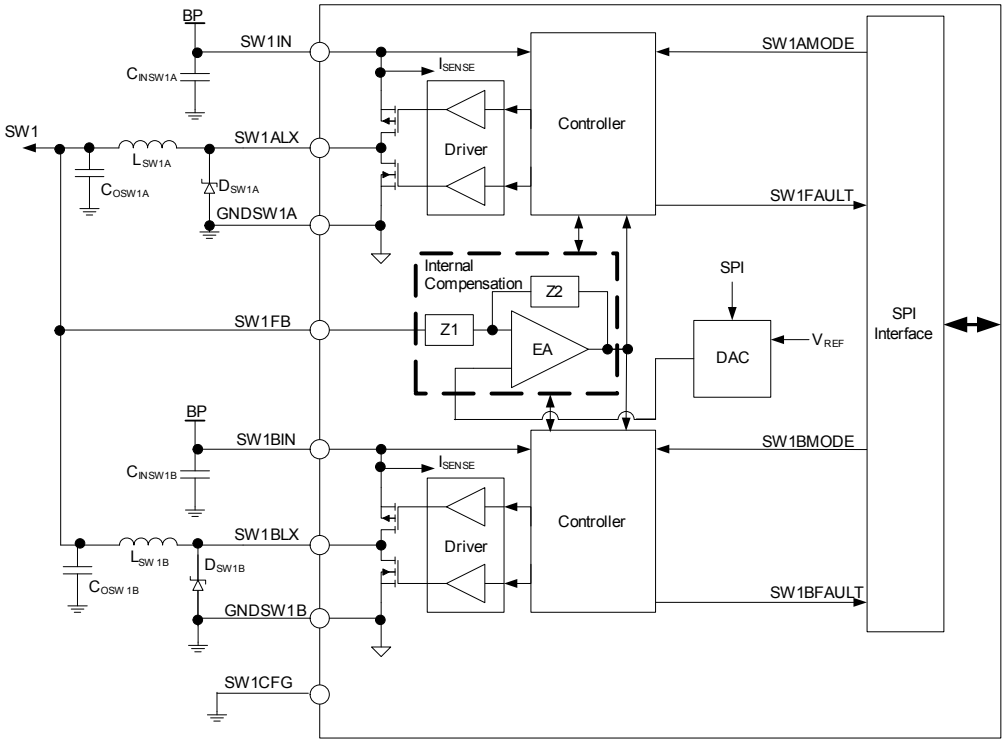


Figure 9. SW1 Dual Phase Output Mode Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW1FAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW1A/B output voltage is SPI configurable in step sizes of 12.5 mV as shown in the table below. The SPI bits SW1A[5:0] set the output voltage for both SW1A and SW1B.

Table 37. SW1A/B Output Voltage Programmability

Set Point	SW1A[5:0]	SW1A/B Output (V)	Set Point	SW1A[5:0]	SW1A/B Output (V)
0	000000	0.6500	32	100000	1.0500
1	000001	0.6625	33	100001	1.0625
2	000010	0.6750	34	100010	1.0750
3	000011	0.6875	35	100011	1.0875
4	000100	0.7000	36	100100	1.1000
5	000101	0.7125	37	100101	1.1125
6	000110	0.7250	38	100110	1.1250
7	000111	0.7375	39	100111	1.1375
8	001000	0.7500	40	101000	1.1500
9	001001	0.7625	41	101001	1.1625
10	001010	0.7750	42	101010	1.1750
11	001011	0.7875	43	101011	1.1875
12	001100	0.8000	44	101100	1.2000

Table 37. SW1A/B Output Voltage Programmability

Set Point	SW1A[5:0]	SW1A/B Output (V)	Set Point	SW1A[5:0]	SW1A/B Output (V)
13	001101	0.8125	45	101101	1.2125
14	001110	0.8250	46	101110	1.2250
15	001111	0.8375	47	101111	1.2375
16	010000	0.8500	48	110000	1.2500
17	010001	0.8625	49	110001	1.2625
18	010010	0.8750	50	110010	1.2750
19	010011	0.8875	51	110011	1.2875
20	010100	0.9000	52	110100	1.3000
21	010101	0.9125	53	110101	1.3125
22	010110	0.9250	54	110110	1.3250
23	010111	0.9375	55	110111	1.3375
24	011000	0.9500	56	111000	1.3500
25	011001	0.9625	57	111001	1.3625
26	011010	0.9750	58	111010	1.3750
27	011011	0.9875	59	111011	1.3875
28	011100	1.0000	60	111100	1.4000
29	011101	1.0125	61	111101	1.4125
30	011110	1.0250	62	111110	1.4250
31	011111	1.0375	63	111111	1.4375

Table 38. SW1A/B Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SW1A/B BUCK REGULATOR						
V_{SW1IN}	Operating Input Voltage				V	
	• PWM operation, 0 < IL < I_{MAX}	3.0	-	4.5		
	• PFM operation, 0 < IL < IL_{MAX}	2.8	-	4.5		
V_{SW1ACC}	Output Voltage Accuracy				mV	(47)
	• PWM mode including ripple, load regulation, and transients	Nom-25	Nom	Nom+25		
	• PFM Mode, including ripple, load regulation, and transients	Nom-25	Nom	Nom+25		
I_{SW1}	Continuous Output Load Current, V_{INMIN} < BP < 4.5 V				mA	
	• PWM mode single/dual phase (parallel)	-	-	2000		
	• SW1 in PFM mode	-	50	-		
$I_{SW1PEAK}$	Current Limiter Peak Current Detection				A	
	• V_{IN} = 3.6 V, Current through Inductor	-	4.0	-		
I_{SW1} TRANSIENT	Transient Load Change				A	
	• 100 mA/µs	-	-	1.0		
$V_{SW1OS-START}$	Start-up Overshoot, IL = 0	-		25	mV	

Table 38. SW1A/B Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
t_{ON-SW1}	Turn-on Time • Enable to 90% of end value IL = 0	-	-	500	µs	
f_{SW1}	Switching Frequency • PLLX = 0 • PLLX = 1	- -	2.0 4.0	- -	MHz	
I_{SW1Q}	Quiescent Current Consumption • APS MODE, IL=0 mA • PFM MODE, IL=0 mA	- -	240 15	- -	µA	
η_{SW1}	Efficiency, • PFM, 0.9 V, 1.0 mA • PWM, 1.1 V, 200 mA • PWM, 1.1 V, 800 mA • PWM, 1.1 V, 1600 mA	- - - -	54 75 81 76	- - - -	%	(48)

Notes:
47. Transient loading for load steps of ILMAX/2.
48. Efficiency numbers at V_{IN} = 3.6 V, excludes the quiescent current

7.5.4.4 SW2

SW2 is fully integrated synchronous Buck PWM voltage-mode control DC/DC regulator.

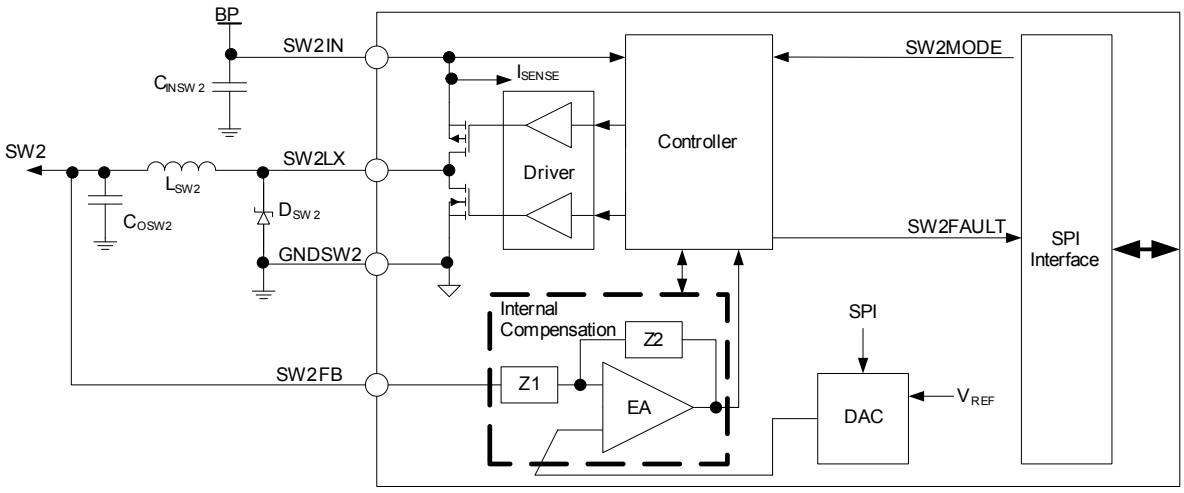


Figure 10. SW2 Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation, alert the system through the SW2FAULT SPI bit, and issue an SCPI interrupt via the INT pin

SW2 can be programmed in step sizes of 12.5 mV as shown in Table 39.

Table 39. SW2 Output Voltage Programmability

Set Point	SW2[5:0]	SW2x Output (V)	Set Point	SW2[5:0]	SW2 Output (V)
0	000000	0.6500	32	100000	1.0500
1	000001	0.6625	33	100001	1.0625
2	000010	0.6750	34	100010	1.0750
3	000011	0.6875	35	100011	1.0875
4	000100	0.7000	36	100100	1.1000
5	000101	0.7125	37	100101	1.1125
6	000110	0.7250	38	100110	1.1250
7	000111	0.7375	39	100111	1.1375
8	001000	0.7500	40	101000	1.1500
9	001001	0.7625	41	101001	1.1625
10	001010	0.7750	42	101010	1.1750
11	001011	0.7875	43	101011	1.1875
12	001100	0.8000	44	101100	1.2000
13	001101	0.8125	45	101101	1.2125
14	001110	0.8250	46	101110	1.2250
15	001111	0.8375	47	101111	1.2375
16	010000	0.8500	48	110000	1.2500
17	010001	0.8625	49	110001	1.2625
18	010010	0.8750	50	110010	1.2750
19	010011	0.8875	51	110011	1.2875
20	010100	0.9000	52	110100	1.3000
21	010101	0.9125	53	110101	1.3125
22	010110	0.9250	54	110110	1.3250
23	010111	0.9375	55	110111	1.3375
24	011000	0.9500	56	111000	1.3500
25	011001	0.9625	57	111001	1.3625
26	011010	0.9750	58	111010	1.3750
27	011011	0.9875	59	111011	1.3875
28	011100	1.0000	60	111100	1.4000
29	011101	1.0125	61	111101	1.4125
30	011110	1.0250	62	111110	1.4250
31	011111	1.0375	63	111111	1.4375

Table 40. SW2 Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SW2 BUCK REGULATOR						
V_{SW2IN}	Operating Input Voltage				V	
	• PWM operation, 0 < IL < I_{MAX}	3.0	-	4.5		
	• PFM operation, 0 < IL < IL_{MAX}	2.8	-	4.5		
V_{SW2ACC}	Output Voltage Accuracy				mV	(49)
	• PWM mode including ripple, load regulation, and transients	Nom-25	Nom	Nom+25		
	• PFM Mode, including ripple, load regulation, and transients	Nom-25	Nom	Nom+25		
I_{SW2}	Continuous Output Load Current, V_{INMIN} < BP < 4.65 V				mA	
	• PWM mode	-	-	1000		
	• PFM mode	-	50	-		
$I_{SW2PEAK}$	Current Limiter Peak Current Detection				A	
	• V_{IN} = 3.6 V Current through Inductor	-	2.0	-		
$I_{SW2\ TRANSIENT}$	Transient Load Change				A	
	• 100 mA/µs	-	-	0.500		
$V_{SW2OS-START}$	Start-up Overshoot, IL = 0	-	-	25	mV	
t_{ON-SW2}	Turn-on Time				µs	
	• Enable to 90% of end value IL = 0	-	-	500		
f_{SW2}	Switching Frequency			-	MHz	
	• PLLX = 0	-	2.0	-		
	• PLLX = 1	-	4.0	-		
I_{SW2Q}	Quiescent Current Consumption				µA	
	• APS MODE, IL = 0 mA; device not switching	-	160	-		
	• PFM MODE, IL = 0 mA; device not switching	-	15	-		
η_{SW2}	Efficiency				%	(50)
	• PFM, 0.9 V, 1.0 mA	-	54	-		
	• PWM, 1.2 V, 120 mA	-	75	-		
	• PWM, 1.2 V, 500 mA	-	83	-		
	• PWM, 1.2 V, 1000 mA	-	78	-		

Notes:

49. Transient loading for load steps of ILMAX/2.
50. Efficiency numbers at V_{IN} = 3.6 V, excludes the quiescent current.

7.5.4.5 SW3

SW3 is fully integrated synchronous Buck PWM voltage mode control DC/DC regulator.

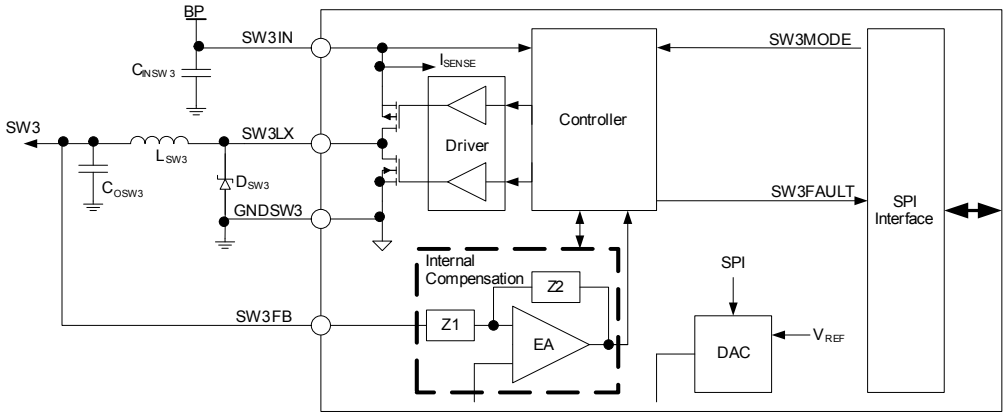


Figure 11. SW3 Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW3FAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW3 can be programmed in step sizes of 25 mV as shown in Table 41.

Table 41. SW3 Output Voltage Programmability

Set Point	SW3[4:0]	SW3 Output (V)	Set Point	SW3[4:0]	SW3 Output (V)
0	00000	0.6500	16	10000	1.0500
1	00001	0.6750	17	10001	1.0750
2	00010	0.7000	18	10010	1.1000
3	00011	0.7250	19	10011	1.1250
4	00100	0.7500	20	10100	1.1500
5	00101	0.7750	21	10101	1.1750
6	00110	0.8000	22	10110	1.2000
7	00111	0.8250	23	10111	1.2250
8	01000	0.8500	24	11000	1.2500
9	01001	0.8750	25	11001	1.2750
10	01010	0.9000	26	11010	1.3000
11	01011	0.9250	27	11011	1.3250
12	01100	0.9500	28	11100	1.3500
13	01101	0.9750	29	11101	1.3750
14	01110	1.0000	30	11110	1.4000
15	01111	1.0250	31	11111	1.4250

Table 42. SW3 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SW3 BUCK REGULATOR						
V_{SW3IN}	Operating Input Voltage				V	
	• PWM operation, 0 < IL < I_{MAX}	3.0	-	4.5		
	• PFM operation, 0 < IL < IL_{MAX}	2.8	-	4.5		
V_{SW3ACC}	Output Voltage Accuracy				mV	(51)
	• PWM mode including ripple, load regulation, and transients	Nom-3%	Nom	Nom+3%		
	• PFM Mode, including ripple, load regulation, and transients	Nom-3%	Nom	Nom+3%		
I_{SW3}	Continuous Output Load Current, V_{INMIN} < BP < 4.65 V				mA	
	• PWM mode	-	-	500		
	• PFM mode	-	50	-		
$I_{SW3PEAK}$	Current Limiter Peak Current Detection				A	
	• V_{IN} = 3.6 V Current through Inductor	-	1.0	-		
$I_{SW3\ TRANSIENT}$	Transient Load Change	-	-	250	mA	
	• 100 mA/µs					
$V_{SW3OS-START}$	Start-up Overshoot, IL = 100 mA/µs	-	-	25	mV	
t_{ON-SW3}	Turn-on Time				µs	
	• Enable to 90% of end value IL = 0	-	-	500		
f_{SW3}	Switching Frequency				MHz	
	• PLLX = 0	-	2.0	-		
	• PLLX = 1	-	4.0	-		
I_{SW3Q}	Quiescent Current Consumption				µA	
	• APSMODE, IL = 0 mA; device not switching	-	160	-		
	• PFM MODE, IL = 0 mA; device not switching	-	15	-		
η_{SW3}	Efficiency,				%	(52)
	• PFM, 1.2 V, 1.0 mA	-	71	-		
	• PWM, 1.2 V, 120 mA	-	79	-		
	• PWM, 1.2 V, 250 mA	-	82	-		
	• PWM, 1.2V, 500 mA	-	81	-		

Notes:

51. Transient loading for load steps of ILMAX/2
52. Efficiency numbers at VIN = 3.6 V, Excludes the quiescent current,

7.5.4.6 SW4

SW4A/B is fully integrated synchronous Buck PWM voltage-mode control DC/DC regulator. It can be operated in (single phase/ dual phase mode) or as separate independent outputs. The operating mode of the Switching regulator is configured by the SW4CFG pin. The SW4CFG pin is sampled at startup.

Table 43. SW4A/B Configuration

SW4CFG	SW4A/B Configuration Mode
Ground	Separate Independent Output
VCOREDIG	Single Phase
VCORE	Dual Phase

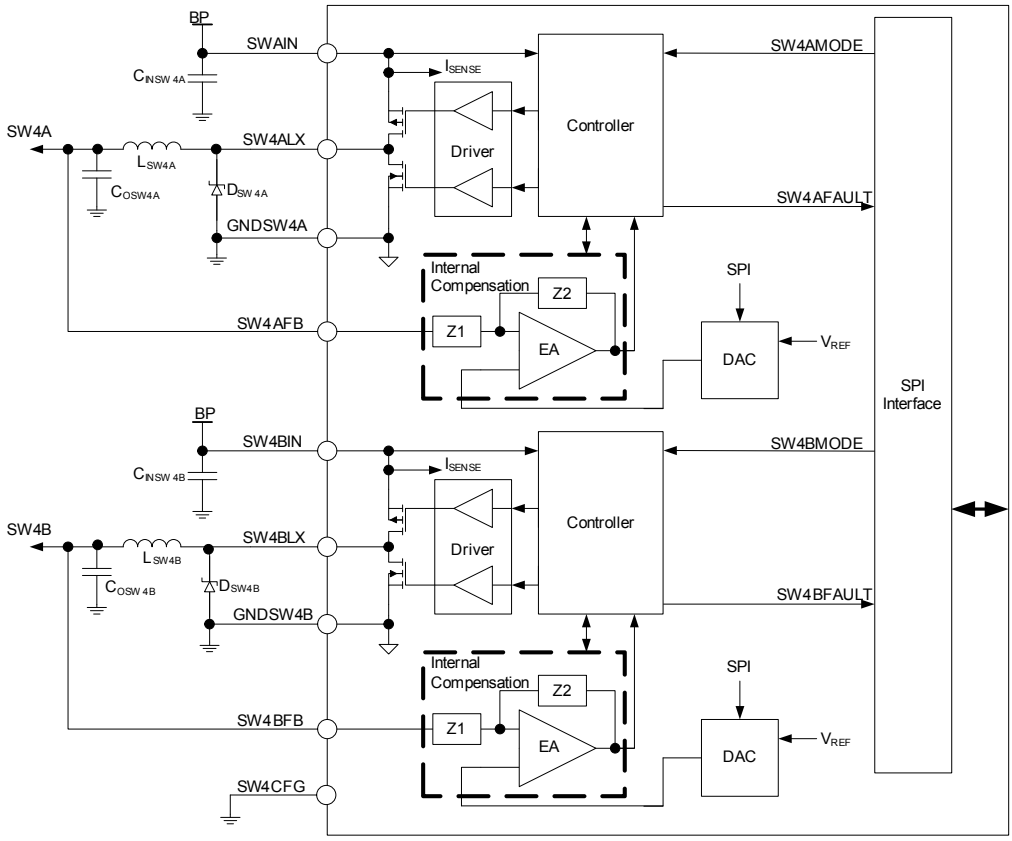


Figure 12. SW4A/B Separate Output Mode Block Diagram

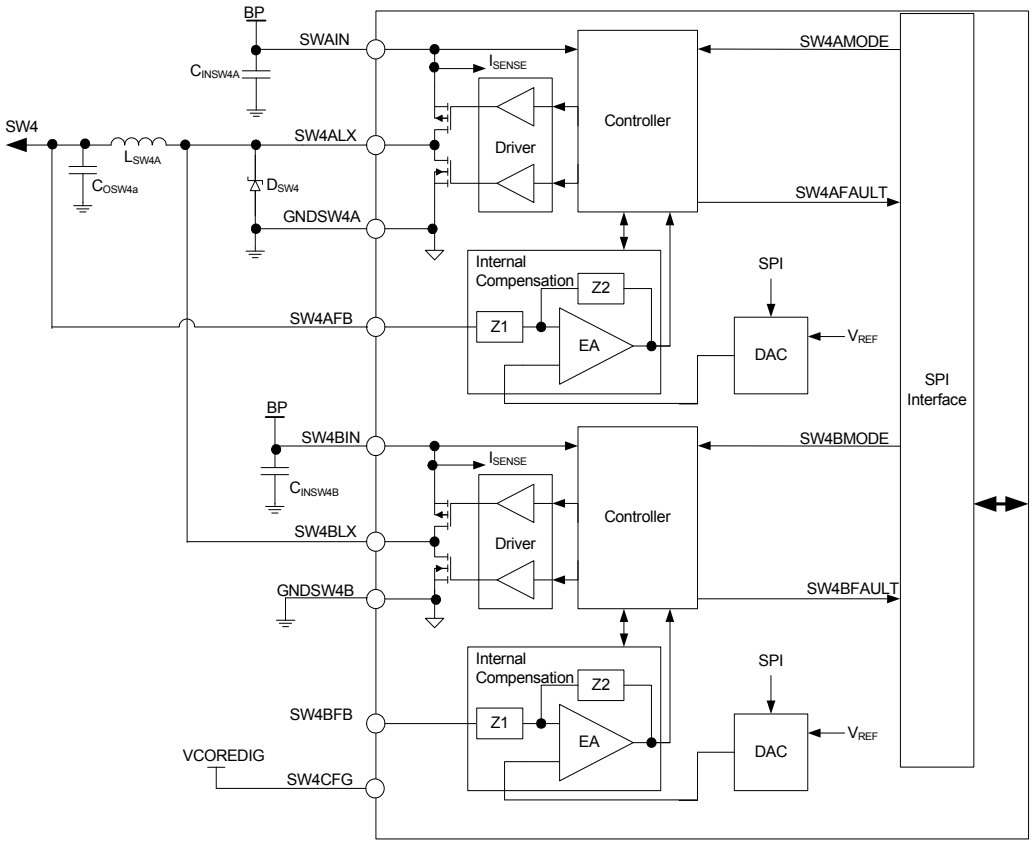


Figure 13. SW4 Single Phase Output Mode Block Diagram

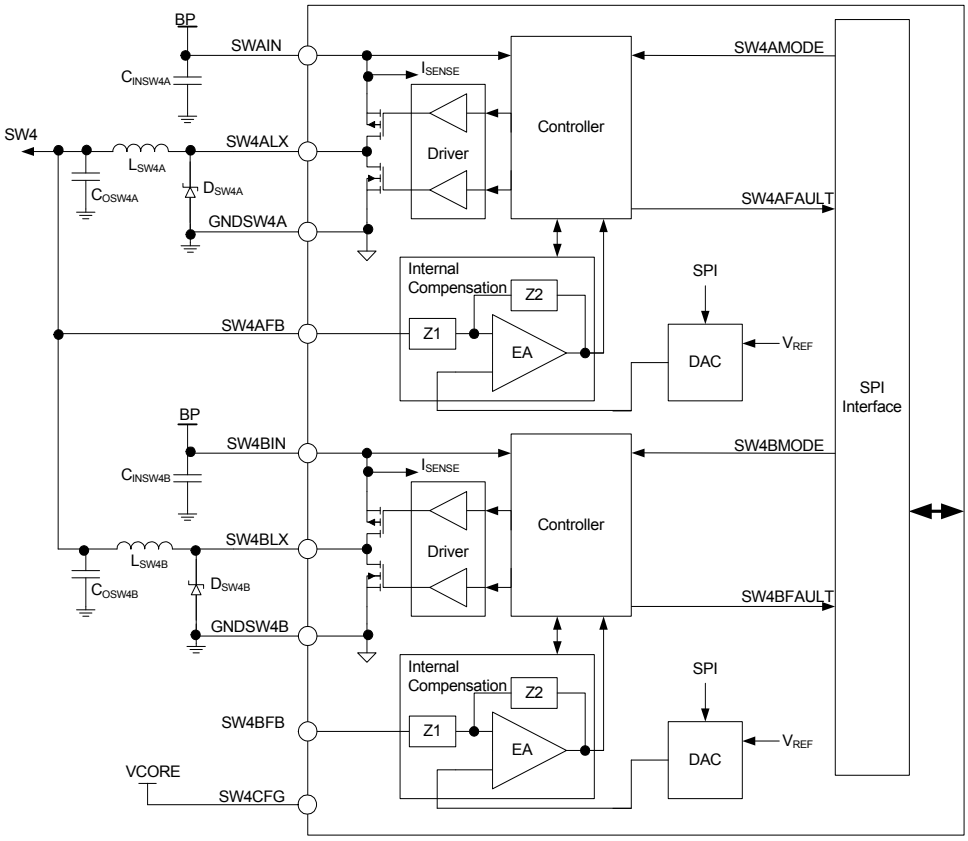


Figure 14. SW4 Dual Phase Output Mode Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW4xFAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW4A/B has a high output range (2.5 V, 3.15 V) and a low output range (1.2 V – 1.85 V). The SW4A/B output range is set by the PUMS configuration at start-up and cannot be changed dynamically by software. This means if the PUMS are set to allow SW4A to come up in the high output voltage range, the output can only be changed between 2.5 V or 3.15 V. It cannot be programmed in the low output range. If software sets the SW4AHI[1:0] = 00 when the PUMS is set to come up in the high voltage range, the output voltage will only go as low as the lowest setting in the high range, which is 2.5 V. If the PUMS are set to start-up in the low output voltage range, the voltage is controlled through the SW4x[4:0] bits by software, it cannot be programmed into the high voltage range. When changing the voltage in either the high or low voltage range, the regulator should be forced into PWM mode to change the voltage.

Table 44. SW4A/B Output Voltage Select

SW4xHI[1:0]	Set point selected by	Output Voltage
00	SW4x[4:0]	See Table 45
01	SW4xHI[1:0]	2.5 V
10	SW4xHI[1:0]	3.15 V
11	Invalid	Invalid

Table 45. SW4A/B Output Voltage Programmability

Set Point	SW4x[4:0]	SW4x Output (V)	Set Point	SW4x[4:0]	SW4x Output (V)
0	00000	1.2000	16	10000	1.6000
1	00001	1.2250	17	10001	1.6250
2	00010	1.2500	18	10010	1.6500
3	00011	1.2750	19	10011	1.6750
4	00100	1.3000	20	10100	1.7000
5	00101	1.3250	21	10101	1.7250
6	00110	1.3500	22	10110	1.7500
7	00111	1.3750	23	10111	1.7750
8	01000	1.4000	24	11000	1.8000
9	01001	1.4250	25	11001	1.8250
10	01010	1.4500	26	11010	1.8500
11	01011	1.4750	-	-	-
12	01100	1.5000	-	-	-
13	01101	1.5250	-	-	-
14	01110	1.5500	-	-	-
15	01111	1.5750	-	-	-

Table 46. SW4A/B Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SW4A/B Buck Regulator						
V_{SW4IN}	Operating Input Voltage				V	(54)
	• PWM operation, 0 < IL < I_{MAX}	3.0	-	4.5		
	• PFM operation, 0 < IL < IL_{MAX}	2.8	-	4.5		
V_{SW4ACC}	Output Voltage Accuracy				mV	(53)
	• PWM mode including ripple, load regulation, and transients	Nom-3%	Nom	Nom+3%		
	• PFM Mode, including ripple, load regulation, and transients	Nom-3%	Nom	Nom+3%		
I_{SW4}	Continuous Output Load Current, V_{INMIN} < BP < 4.5 V				mA	
	• PWM mode (separate)	-	-	500		
	• PWM mode single/dual phase	-	-	1000		
	• PFM mode	-	50	-		
$I_{SW4PEAK}$	Current Limiter Peak Current Detection				A	
	• V_{IN} = 3.6 V Current through Inductor (separate)	-	1.0	-		
	• Current through Inductor	-	2.0	-		
$i_{SW4\ TRANSIENT}$	Transient Load Change, 100 mA/µs				mA	
	• Single/Dual Phase	-	-	500		
	• Separate	-	-	250		
$V_{SW4OS-START}$	Start-up Overshoot, IL = 100 mA/µs	-	-	25	mV	

Table 46. SW4A/B Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
t_{ON-SW4}	Turn-on Time • Enable to 90% of end value IL = 0	- -	- -	- 500	µs	
f_{SW4}	Switching Frequency • PLLX = 0 • PLLX = 1	- -	- 2.0 4.0	- - -	MHz	
I_{SW4Q}	Quiescent Current Consumption • APS MODE, IL = 0 mA; High output voltage range (V_{SW4x} = 3.15 V or 2.5 V) device not switching • APS MODE, IL = 0 mA; Low output voltage range (V_{SW4x} = 1.3 V). device not switching • PFM MODE, IL = 0 mA; device not switching	- - -	- 500 260 15	- - - -	µA	
η_{SW4}	Efficiency • PFM, 3.15 V, 10 mA (A) • PWM, 3.15 V, 50 mA (A) • PWM, 3.15 V, 250 mA (A) • PWM, 3.15 V, 500 mA (A) • PFM, 1.2 V, 10 mA (B) • PWM, 1.2 V, 50 mA (B) • PWM, 1.2 V, 250 mA (B) • PWM 1.2 V, 500 mA (B)	- - - - - - - -	- 79 93 92 82 72 71 81 78	- - - - - - - - -	%	(55)

Notes:

53. Transient loading for load steps of IL_{MAX} / 2.
54. When SW4A/B is set to 3.0 V and above the regulator may drop out of regulation when BP nears the output voltage.
55. Efficiency numbers at V_{IN} = 3.6 V, excludes the quiescent current.

7.5.4.7 SW5

SW5 is fully integrated synchronous Buck PWM voltage mode control DC/DC regulator.

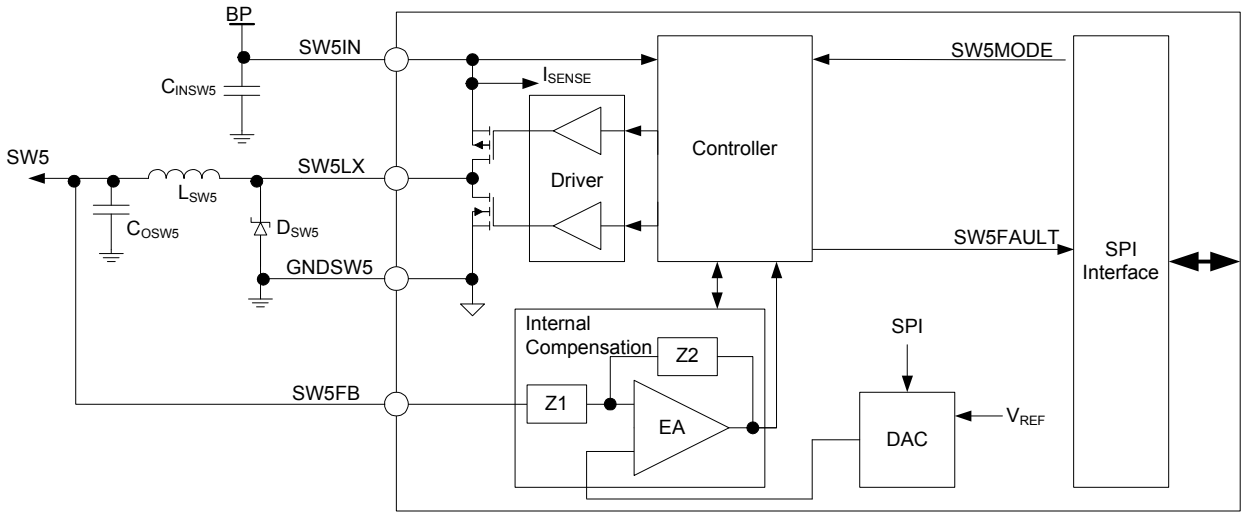


Figure 15. SW5 Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW5FAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW5 can be programmed in step sizes of 25 mV as shown in Table 47. If the software wants to change the output voltage, after power up the regulator should be forced into PWM mode to change the voltage.

Table 47. SW5 Output Voltage Programmability

Set Point	SW5[4:0]	SW5 Output (V)	Set Point	SW5[4:0]	SW5 Output (V)
0	00000	1.2000	16	10000	1.6000
1	00001	1.2250	17	10001	1.6250
2	00010	1.2500	18	10010	1.6500
3	00011	1.2750	19	10011	1.6750
4	00100	1.3000	20	10100	1.7000
5	00101	1.3250	21	10101	1.7250
6	00110	1.3500	22	10110	1.7500
7	00111	1.3750	23	10111	1.7750
8	01000	1.4000	24	11000	1.8000
9	01001	1.4250	25	11001	1.8250
10	01010	1.4500	26	11010	1.8500
11	01011	1.4750	-	-	-
12	01100	1.5000	-	-	-
13	01101	1.5250	-	-	-
14	01110	1.5500	-	-	-
15	01111	1.5750	-	-	-

Table 48. SW5 Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SW5 BUCK REGULATOR						
V_{SW5IN}	Operating Input Voltage				V	
	• PWM operation, 0 < IL < I_{MAX}	3.0	-	4.5		
	• PFM operation, 0 < IL < IL_{MAX}	2.8	-	4.5		
V_{SW5ACC}	Output Voltage Accuracy				mV	(56)
	• PWM mode including ripple, load regulation, and transients	Nom-3%	Nom	Nom+3%		
	• PFM Mode, including ripple, load regulation, and transients	Nom-3%	Nom	Nom+3%		
I_{SW5}	Continuous Output Load Current, V_{INMIN} < BP < 4.5 V				mA	
	• PWM mode	-	-	1000		
	• PFM mode	-	50	-		
$I_{SW5PEAK}$	Current Limiter Peak Current Detection				A	
	• V_{IN} = 3.6 V Current through Inductor	-	1.0	-		
I_{SW5} TRANSIENT	Transient Load Change				mA	
	• 100 mA/µs	-	-	500		
V_{SW5} OS-START	Start-up Overshoot, IL = 0	-	-	25	mV	
t_{ON-SW5}	Turn-on Time				µs	
	• Enable to 90% of end value IL = 0	-	-	500		
f_{SW5}	Switching Frequency				MHz	
	• PLLX = 0	-	2.0	-		
	• PLLX = 1	-	4.0	-		
I_{SW5Q}	Quiescent Current Consumption				µA	
	• APS MODE, IL = 0 mA; device not switching	-	160	-		
	• PFM MODE, IL = 0 mA; device not switching	-	15	-		
η_{SW5}	Efficiency				%	(57)
	• PFM, 1.8 V, 1.0 mA	-	80	-		
	• PWM, 1.8 V, 50 mA	-	79	-		
	• PWM, 1.8 V, 500 mA	-	86	-		
	• PWM, 1.8 V, 1000 mA	-	82	-		

Notes

56. Transient Loading for load Steps of ILMAX/2
57. Efficiency numbers at VIN = 3.6 V, Excludes the quiescent current.

7.5.4.8 Dynamic Voltage Scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor. SW1A/B and SW2 allow for two different set points with controlled transitions to avoid sudden output voltage changes, which could cause logic disruptions on their loads.

Preset operating points for SW1A/B and SW2 can be set up for:

- Normal operation: output value selected by SPI bits SWx[5:0]. Voltage transitions initiated by SPI writes to SWx[5:0] are governed by the DVS stepping rate shown in the following tables.
- Standby (Deep Sleep): can be higher or lower than normal operation, but is typically selected to be the lowest state retention voltage of a given process. Set by SPI bits SWxSTBY[5:0] and controlled by a Standby event. Voltage transitions initiated by Standby are governed by the SWxDVSSPEED[1:0] SPI bits shown in Table 49.

  The following table summarizes the set point control and DVS time stepping applied to SW1A/B and SW2.

Table 49. DVS Control Logic Table for SW1A/B and SW2

STANDBY	Set Point Selected by
0	SWx[4:0]
1	SWxSTBY[4:0]

Table 50. DVS Speed Selection

SWxDVSSPEED[1:0]	Function
00	12.5 mV step each 2.0 μs
01 (default)	12.5 mV step each 4.0 μs
10	12.5 mV step each 8.0 μs
11	12.5 mV step each 16.0 μs

The regulators have a strong sourcing and sinking capability in the PWM mode. Therefore, the rising/falling slope is determined by the regulator in PWM mode, however, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Voltage transitions programmed through SPI(SWx[4:0]) on SW3 and SW5 will step in increments of 25 mV per 4.0 μs, SW4A/B will step in increments of 25 mV per 8.0 μs when SW4xHI[1:0]=00, and SW4A/B will step in increments of 25 mV per 16 μs when SW4xHI[1:0]=00. Additionally, SW3, SW4/B, and SW5 include standby mode set point programmability.

The following diagram shows the general behavior for the switching regulators when initiated with SPI programming or standby control.

SW1 and SW2 also contain power good outputs to the application processor. The power good signal is an active high signal. When SWxPWGD is high, it means the regulator's output has reached its programmed voltage. The SWxPWGD voltage outputs will be low during the DVS period and if the current limit is reached on the switching regulator. During the DVS period, the over-current condition on the switching regulator should be masked. If the current limit is reached outside of a DVS period, the SWxPWGD pin will stay low until the current limit condition is removed.

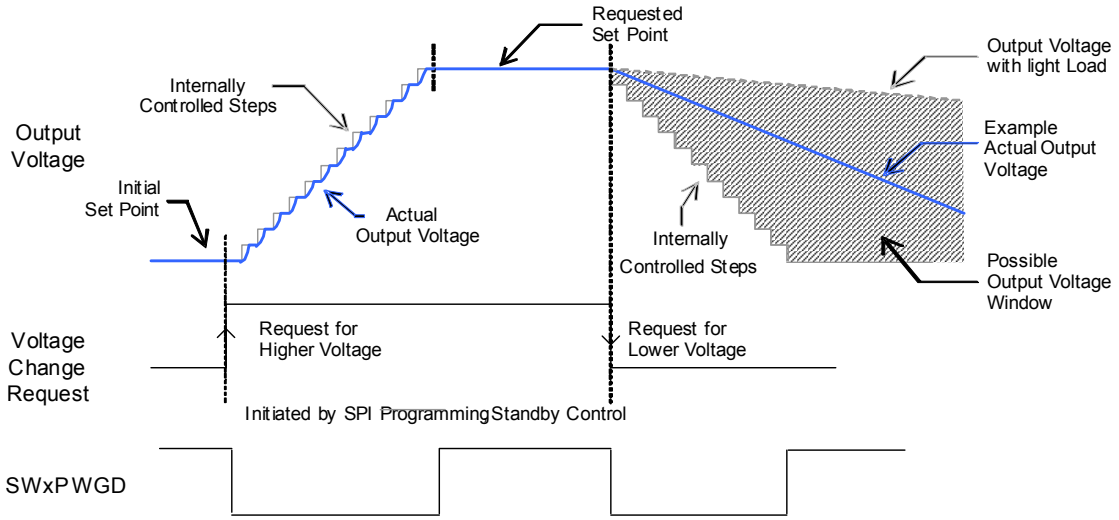


Figure 16. Voltage Stepping with DVS

7.5.5 Boost Switching Regulator

SWBST is a boost switching regulator with a programmable output, which defaults to 5.0 V on power up, operating at 2.0 MHz. SWBST supplies the VUSB regulator for the USB PHY in OTG mode, as well as the VBUS voltage. Note that the parasitic leakage path for a boost regulator will cause the output voltage and SWBSTFB to sit at a Schottky drop below the battery voltage whenever SWBST is disabled. The switching NMOS transistor is integrated on-chip. An external fly back Schottky diode, inductor, and capacitor are required.

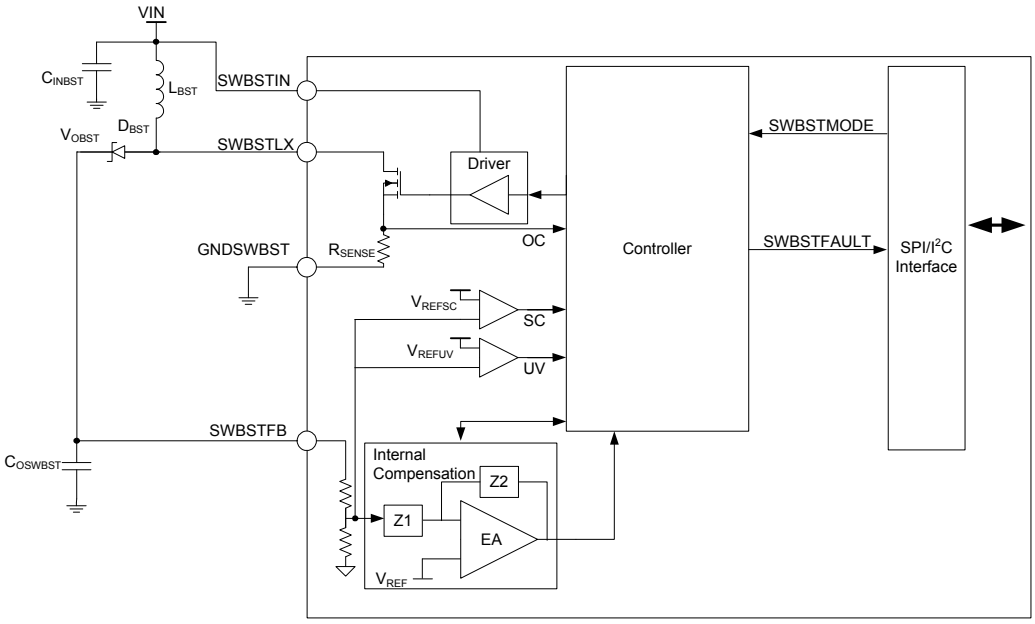


Figure 17. Boost Regulator Architecture

SWBST output voltage programmable via the SWBST[1:0] SPI bits as shown in Table 51.

Table 51. SWBST Voltage Programming

Parameter	Voltage	SWBST Output Voltage
SWBST[1:0]	00	5.000 (default)
	01	5.050
	10	5.100
	11	5.150

SWBST can be controlled by SPI programming in PFM, APS, and Auto mode. Auto mode transitions between PFM and APS mode based on the load current. By default SWBST is powered up in Auto mode.

Table 52. SWBST Mode Control

Parameter	Voltage	SWBST Mode
SWBSTMODE[1:0] SWBSTSTBYMODE[1:0]	00	Off
	01	PFM
	10	Auto (default)
	11	APS

Table 53. SWBST Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SWITCH MODE SUPPLY SWBST						
V_{SWBST}	Average Output Voltage • 3.0 V < V_{IN} < 4.5 V, 0 < IL < IL_{MAX}	Nom-4%	V_{NOM}	Nom+3%	V	(58)
$V_{SWBSTACC}$	Output Ripple • 3.0 V < V_{IN} < 4.5 V 0 < IL < IL_{MAX}, excluding reverse recovery of Schottky diode	-	-	120 mV	Vp-p	
$SWBST_{ACC}$	Average Load Regulation • V_{IN} = 3.6 V, 0 < IL < IL_{MAX}	-	0.5	-	mV/mA	
$V_{SWBST\ LINEAREG}$	Average Line Regulation • 3.0 V < V_{IN} < 4.5 V IL = IL_{MAX}	-	50	-	mV	
I_{SWBST}	Continuous Load Current • 3.0 V < V_{IN} < 4.5 V, V_{OUT} = 5.0 V	-	380	-	mA	
$I_{SWBSTPEAK}$	Peak Current Limit • At SWBSTIN, V_{IN} = 3.6 V	-	1800	-	mA	
$V_{SWBSTOS-START}$	Start-up Overshoot, IL = 0 mA	-	-	500	mV	
$t_{ON-SWBST}$	Turn-on Time • Enable to 90% of V_{OUT} IL = 0	-	-	2.0	ms	
f_{SWBST}	Switching Frequency	-	2.0	-	MHz	
$V_{SWBST\ TRANSIENT}$	Transient Load Response, IL from 1.0 to 100 mA in 1.0 µs • Maximum transient Amplitude	-	-	300	mV	

Table 53. SWBST Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
$V_{SWBST\ TRANSIENT}$	Transient Load Response, IL from 100 to 1.0 mA in 1.0 µs • Maximum transient Amplitude	-	-	300	mV	
$V_{SWBST\ TRANSIENT}$	Transient Load Response, IL from 1.0 to 100 mA in 1.0 µs • Time to settle 80% of transient	-	-	500	µs	
$V_{SWBST\ TRANSIENT}$	Transient Load Response, IL from 100 to 1.0 mA in 1.0 µs • Time to settle 80% of transient	-	-	20	ms	
η_{SWBST}	Efficiency, IL = IL_{MAX}	65	80	-	%	
$I_{SWBSTBIAS}$	Bias Current Consumption • PFM or Auto mode	-	35	-	µA	
$I_{LEAK-SWBST}$	NMOS Off Leakage • SWBSTIN = 4.5 V, SWBSTMODE [1:0] = 0	-	1.0	6.0	µA	

Notes:

58. V_{IN} is the low side of the inductor connected to BP.

7.5.6 Linear Regulators (LDOs)

This section describes the linear regulators provided. For convenience, these regulators are named to indicate their typical or possible applications, but the supplies are not limited to these uses and may be applied to any loads within the specified regulator capabilities.

A low power standby mode controlled by STANDBY is provided for the regulators with an external pass device in which the bias current is aggressively reduced. This mode is useful for deep sleep operation, where certain supplies cannot be disabled, but active regulation can be tolerated with lesser parametric requirements. The output drive capability and performance are limited in this mode.

7.5.6.1 General Guidelines

The following applies to all linear regulators, unless otherwise specified.

- Parametric specifications assume the use of low ESR X5R/X7R ceramic capacitors with 20% accuracy and 15% temperature spread, for a worst case stack up of 35% from the nominal value. Use of other types with wider temperature variation may require a larger room temperature nominal capacitance value, to meet performance specs over temperature. Capacitor derating as a function of DC bias voltage requires special attention. Minimum bypass capacitor guidelines are provided for stability and transient performance. However, larger values may be applied, but performance metrics may be altered and generally improved and should be confirmed in system applications.
- Regulators with an external PNP transistor require an equivalent resistance (including the ESR) in series with the output capacitor, as noted in the specific regulator sections.
- Output voltage tolerance specified for each of the linear regulators include process variation, temperature range, static line regulation, and static load regulation.
- In the Low-power mode, the output performance is degraded. Only those parameters listed in the Low-power mode section are guaranteed. In this mode, the output current is limited to much lower levels than in the active mode.
- When a regulator gets disabled, the output will be pulled to ground by an internal pull-down. The pull-down is also activated when RESETB goes low.

7.5.6.2 LDO Regulator Control

The regulators with embedded pass devices (VPLL, VGEN1, and VUSB) have an adaptive biasing scheme thus, there are no distinct operating modes such as a Normal mode and a Low Power mode. Therefore, no specific control is required to put these regulators in a Low Power mode.

The external pass regulator (VDAC) can also operate in a normal and low power mode. However, since a load current detection cannot be performed for this regulator, the transition between both modes is not automatic and is controlled by setting the corresponding mode bits for the operational behavior desired.

The regulators VUSB2, and VGEN2 can be configured for using the internal pass device or external pass device as explained in Supplies. For both configurations, the transition between both modes is controlled by setting the VxMODE bit for the specific regulator. Therefore, depending on the configuration selected, the automatic Low Power mode determines availability.

The regulators can be disabled and the general purpose outputs can be forced low when going into Standby (note that the Standby response timing can be altered with the STBYDLY function, as described in the previous section). Each regulator has an associated SPI bit for this. When the bit is not set, STANDBY is of no influence. The actual operating mode of the regulators as a function of STANDBY is not reflected through SPI. In other words, the SPI will read back what is programmed, not the actual state.

Table 54. LDO Regulator Control (external pass device LDOs)

VxEN	VxMODE	VxSTBY	STANDBY[59]	Regulator Vx
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low Power
1	X	1	0	On
1	0	1	1	Off
1	1	1	1	Low Power

Notes
59. STANDBY refers to a Standby event as described earlier

For regulators with internal pass devices, the previous table can be simplified by elimination of the VxMODE column.

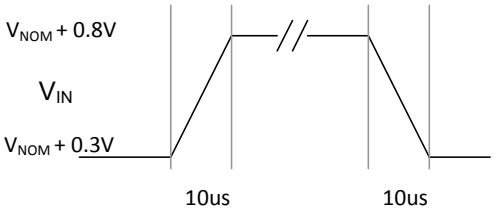
Table 55. LDO Regulator Control (internal pass device LDOs)

VxEN	VxSTBY	STANDBY [60]	Regulator Vx
0	X	X	Off
1	0	X	On
1	1	0	On
1	1	1	Off

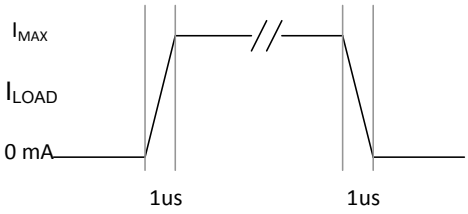
Notes
60. STANDBY refers to a Standby event as described earlier

7.5.6.3 Transient Response Waveforms

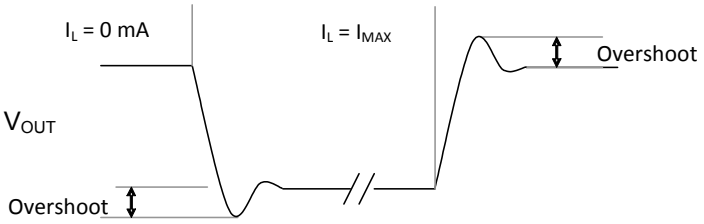
The transient load and line response are specified with the waveforms as depicted in Figure 18. Note that where the transient load response refers to the overshoot only, so excluding the DC shift itself, the transient line response refers to the sum of both overshoot and DC shift. This is also valid for the mode transition response.



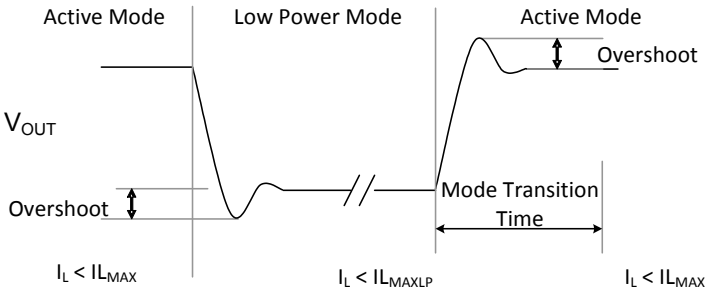
V_{IN} Stimulus for Transient Line Response



I_{LOAD} Stimulus for Transient Load Response



V_{OUT} for Transient Load Response



V_{OUT} for Mode Transition Response
(V_{GEN2}, V_{USB2}, V_{DAC})

Figure 18. Transient Waveforms

7.5.6.4 Short-circuit Protection

The higher current LDOs, and those most accessible in product applications, include a short-circuit detection and protection (VDAC, VUSB, VUSB2, VGEN1, and VGEN2). The short-circuit protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If an over-current (short-circuit) condition is detected, typically 20% above I_{LMAX}, the LDO will be disabled by resetting its VxEN bit, while at the same time, an interrupt SCPI will be generated to flag the fault to the system processor. The SCPI interrupt is maskable through the SCPM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, then not only is no interrupt generated, but also the regulators will not automatically be disabled upon a short-circuit detection. Note that by default, the REGSCPEN bit is not set, so at startup, none of the regulators in an overload condition are disabled.

7.5.6.5 VPLL

VPLL is provided for isolated biasing of the application processors PLLs for clock generation, in support of protocol and peripheral needs. Depending on the application and power requirements, this supply may be considered for sharing with other loads, but

noise injection must be avoided and filtering added, if necessary to ensure suitable PLL performance. The VPLL regulator has a dedicated input supply pin.

VINPLL can be connected to either BP or a 1.8 V switched mode power supply rail such as from SW5 for the two lower set points of each regulator VPLL[1:0] = [00], [01]. In addition, when the two upper set points (VPLL[1:0] = [10],[11]) are used, the VINPLL inputs can be connected to either BP or a 2.2 V nominal external switched mode power supply rail, to improve power dissipation.

Table 56. VPLL Voltage Control

Parameter	Value	Function	ILoad max	Input Supply
VPLL[1:0]	00	output = 1.2 V	50 mA	BP or 1.8 V
	01	output = 1.25 V	50 mA	BP or 1.8 V
	10	output = 1.50 V	50 mA	BP or External switch
	11	output = 1.8 V	50 mA	BP or External switch

Table 57. VPLL Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V,-40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
GENERAL						
V_{INPLL}	Operating Input Voltage Range				V	
	• VPLL all settings, BP biased	UVDET	-	4.5		
	• VPLL [1:0] = 00, 01 (SW5 = 1.8 V)	1.75	1.8	4.5		
	• VPLL, [1:0] = 10, 11, External Switch	2.15	2.2	4.5		
I_{PLL}	Operating current Load range	-	-	50	mA	
VPLL ACTIVE MODE – DC						
V_{PLL}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$, • $IL_{MIN} < IL < IL_{MAX}$	V_{NOM} – 0.05	V_{NOM}	V_{NOM} + 0.05	V	
$V_{PLL-LOPP}$	Load Regulation • 1.0 mA < IL < IL_{MAX} For any $V_{INMIN} < V_{IN} < V_{INMAX}$	-	0.35	-	mV/mA	
$V_{PLL-LIPP}$	Line Regulation • $V_{INMIN} < V_{IN} < V_{INMAX}$ For any $IL_{MIN} < IL < IL_{MAX}$	-	5.0	-	mV	
I_{PLL-Q}	Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	8.0	-	µA	
VPLL ACTIVE MODE – AC						
$VPLL_{PSRR}$	PSRR, IL = 75% of IL_{MAX}, 20 Hz to 20 kHz				dB	
	• V_{IN} = UVDET	-	70	-		
	• $V_{IN} = V_{NOM}$ + 1.0 V, > UVDET	-	75	-		
$t_{ON-VPLL}$	Turn-on Time • Enable to 90% of end value $V_{IN} = V_{INMIN}$, V_{INMAX} IL = 0	-	-	120	µs	
$t_{OFF-VPLL}$	Turn-off Time • Disable to 10% of initial value $V_{IN} = V_{INMIN}$, V_{INMAX}, IL = 0	0.05	-	10	ms	
$VPLL_{OS-START}$	Start-up Overshoot • $V_{IN} = V_{INMIN}$, V_{INMAX} IL = 0	-	1.0	2.0	%	

Table 57. VPLL Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V,-40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
$V_{PLL-LO\ TRANSIENT}$	Transient Load Response • V_{IN} = V_{INMIN}, V_{INMAX}	-	50	70	mV	
$V_{PLL-LI\ TRANSIENT}$	Transient Line Response • IL = 75% of IL_{MAX}	-	5.0	8.0	mV	

7.5.6.6 VREFDDR

VREFDDR is an internal PMOS half supply Voltage Follower. The output voltage is at one half the input voltage. It's typical application is as the V_{REF} for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

Table 58. VREFDDR Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
GENERAL						
$V_{REFFDDRIN}$	Operating Input Voltage Range V_{INMIN} to V_{INMAX}	1.2	-	1.8	V	
I_{REFDDR}	Operating Current Load Range IL_{MIN} to IL_{MAX}	0.0	-	10	mA	
VREFDDR ACTIVE MODE – DC						
V_{REFDDR}	Output Voltage V_{OUT} • V_{INMIN} < V_{IN} < V_{INMAX} IL_{MIN} < IL < IL_{MAX}	-	V_{IN}/2	-	V	
$V_{REFDDRTOL}$	Output Voltage tolerance • V_{INMIN} < V_{IN} < V_{INMAX} IL = 1.0 mA	-6.5	-	6.5	%	(61)
$V_{REFDDR\ LOPP}$	Load Regulation • 1.0 mA < IL < IL_{MAX} For any V_{INMIN} < V_{IN} < V_{INMAX}	-	5.0	-	mV/mA	
$I_{REFDDRQ}$	Quiescent Current • V_{INMIN} < V_{IN} < V_{INMAX} IL = 0	-	8.0	-	µA	
VREFDDR ACTIVE MODE – AC						
$t_{ON-VREFDDR}$	Turn-on Time • Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	-	-	100	µs	
$t_{OFF-VREFDDR}$	Turn-off Time • Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	0.05	-	10	ms	
$V_{REFDDROS}$	Start-up Overshoot • V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	-	1.0	2.0	%	
$V_{REFDDRL\ TRANSIENT}$	Transient Load Response • V_{IN} = V_{INMIN}, V_{INMAX}	-	5.0	-	mV	

Notes

61. ±2.0% guaranteed at 25 °C only

7.5.6.7 VUSB2

VUSB2 has an internal PMOS pass FET which will support loads up to 65 mA. To support load currents an external PNP is provided. The external PNP configuration is offered to avoid excess on-chip power dissipation at higher loads and large differentials between BP and output settings. For lower current requirements, an integrated PMOS pass FET is included. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option. The external PNP configuration must be committed as a hardwired board level implementation. The recommended PNP device is the ON Semiconductor™ NSS12100XV6T1G, which is capable of handling up to 250 mW of continuous dissipation, at minimum footprint and 75 °C of ambient. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is ON Semiconductor NSS12100UW3TCG. For stability reasons, a total resistance of 50 mΩ ±20% in series with the output capacitance is required. The total resistance includes the ESR of the capacitor plus an external resistance provided by a discrete resistor or PCB circuit trace.

A short-circuit condition will shut down the VUSB2 regulator and generate an interrupt for SCPI, if REGSCPEN is set.

The nominal output voltage of this regulator is SPI configurable, and can be 2.5 V, 2.6 V, 2.75 V, or 3.0 V. The output current when working with the internal pass FET is 65 mA, and could be up to 350 mA when working with an external PNP.

Table 59. VUSB2 Voltage Control

Parameter	Value	Output Voltage	ILoad max	
			VUSB2CONFIG = 0 Internal Pass FET	VUSB2CONFIG = 1 External PNP
VUSB2[1:0]	00	2.5 V	65 mA	350 mA
	01	2.6 V	65 mA	350 mA
	10	2.75 V	65 mA	350 mA
	11	3.00 V	65 mA	350 mA

Table 60. VUSB2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
GENERAL						
V_{USB2IN}	Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{NOM} + 0.25	-	4.5	V	
I_{USB2}	Operating Current Load Range IL_{MIN} to IL_{MAX}				mA	
	• Internal pass FET	0.0	-	65		
	• External PNP Not exceeding PNP max power	0.0	-	350		
V_{USB2IN}	Extended Input Voltage Range				V	
	• Performance may be out of specification	UVDET	-	4.5		
VUSB2 ACTIVE MODE - DC						
V_{USB2}	Output Voltage V_{OUT}				V	
	• $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%		
$V_{USB2LOPP}$	Load Regulation				mV/mA	
	• 1.0 mA < IL < IL_{MAX} For any $V_{INMIN} < V_{IN} < V_{INMAX}$	-	0.25	-		
$V_{USB2LIPP}$	Line Regulation				mV	
	• $V_{INMIN} < V_{IN} < V_{INMAX}$ For any $IL_{MIN} < IL < IL_{MAX}$	-	8.0	-		
I_{USB2Q}	Active Mode Quiescent Current, $V_{INMIN} < V_{IN} < V_{INMAX}$				µA	
	• IL = 0, Internal PMOS configuration	-	25	-		
	• $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0, External PNP configuration	-	30	-		

MC34708

Table 60. VUSB2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VUSB2 LOW POWER MODE - DC						
V_{USB2}	Output Voltage V_{OUT} • V_{INMIN} < V_{IN} < V_{INMAX} IL_{MINLP} < IL < IL_{MAXLP}	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V	
I_{USB2}	Current Load Range IL_{MINLP} to IL_{MAXLP}	0.0	-	3.0	mA	
I_{USB2Q}	Low Power Mode Quiescent Current • V_{INMIN} < V_{IN} < V_{INMAX} IL = 0	-	8.0	10.5	µA	
VUSB2 ACTIVE MODE - AC						
$VUSB2_{PSRR}$	PSRR, IL = 75% of IL_{MAX} 20 Hz to 20 kHz • V_{IN} = V_{INMIN} + 100 mV • V_{IN} = V_{NOM} + 1.0 V	- -	30 30	- -	dB	
$t_{ON-VUSB2}$	Turn-on Time • Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	-	-	1.0	ms	
$t_{OFF-VUSB2}$	Turn-off Time • Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	0.05	-	10	ms	
$VUSB2_{OS-START}$	Start-up Overshoot • V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	-	1.0	2.0	%	
$VUSB2_{LO\ TRANSIENT}$	Transient Load Response, V_{IN} = V_{INMIN}, V_{INMAX}x • VUSB2=01, 10, 11 • VUSB2=00	- -	1.0 50	2.0 70	% mV	
$VUSB2_{LI\ TRANSIENT}$	Transient Line Response • IL = 75% of IL_{MAX}	-	5.0	8.0	mV	
$t_{MOD-VUSB2}$	Mode Transition Time • From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX} IL = IL_{MAXLP}	-	-	100	µs	
$VUSB_{MODE\ RES}$	Mode Transition Response • From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX} IL = IL_{MAXLP}	-	1.0	2.0	%	

7.5.6.8 VDAC

The primary applications of this power supply is the TV-DAC. However, these supplies could also be used for other peripherals if one of these functions is not required. Low Power modes and programmable standby options can be used to optimize power efficiency during deep sleep modes.

An external PNP is utilized for VDAC to avoid excess on-chip power dissipation at high loads and large differentials between BP and output settings. External PNP devices must always be connected to the BP line in the application. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G, which is capable of handling up to 250 mW of continuous dissipation at minimum footprint and 75 °C of ambient. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is ON Semiconductor NSS12100UW3TCG. For stability reasons, a total resistance of 100 mΩ ±20% in series with the output capacitance is required. The total resistance includes the ESR of the capacitor plus an external resistance provided by a discrete resistor or PCB circuit trace.

A short-circuit condition will shut down the VDAC regulator and generate an interrupt for SCPI, if the REGSCPEN bit is set.

The nominal output voltage of this regulator is SPI configurable, and can be 2.5 V, 2.6 V, 2.7 V, or 2.775 V. The maximum output current along with an external PNP, is 250 mA.

Table 61. VDAC Voltage Control

Parameter	Value	Output Voltage	ILoad max
VDAC	00	2.500 V	250 mA
	01	2.600 V	250 mA
	10	2.700 V	250 mA
	11	2.775 V	250 mA

Table 62. VDAC Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
GENERAL						
V_{DACIN}	Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{NOM} + 0.25	-	4.5	V	
I_{DAC}	Operating Current Load Range IL_{MIN} to IL_{MAX} • Not exceeding PNP max power	0.0	-	250	mA	
V_{DACIN}	Extended Input Voltage Range • Performance may be out of specification	UVDET	-	4.5	V	
VDAC ACTIVE MODE – DC						
V_{DAC}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V	
$V_{DACLOPP}$	Load Regulation • 1.0 mA < IL < IL_{MAX} For any $V_{INMIN} < V_{IN} < V_{INMAX}$	-	0.20	-	mV/mA	
$V_{DACLIPP}$	Line Regulation • $V_{INMIN} < V_{IN} < V_{INMAX}$ For any $IL_{MIN} < IL < IL_{MAX}$	-	5.0	-	mV	
I_{DACQ}	Active Mode Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	30	-	µA	
VDAC LOW POWER MODE – DC - VDACMODE=1						
V_{DAC}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MINLP} < IL < IL_{MAXLP}$	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V	
I_{DAC}	Current Load Range IL_{MINLP} to IL_{MAXLP}	0.0	-	3.0	mA	
I_{DACQ}	Low Power Mode Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	8.0	-	µA	
VDAC ACTIVE MODE – AC						
$VDAC_{PSRR}$	PSRR - IL = 75% of IL_{MAX} 20 Hz to 20 kHz • $V_{IN} = V_{INMIN}$ + 100 mV • $V_{IN} = V_{NOM}$ + 1.0 V	- -	50 50	- -	dB	
$t_{ON-VDAC}$	Turn-on Time • Enable to 90% of end value $V_{IN} = V_{INMIN}$, V_{INMAX} IL = 0	-	-	1.0	ms	
$t_{OFF-VDAC}$	Turn-off Time • Disable to 10% of initial value $V_{IN} = V_{INMIN}$, V_{INMAX}, IL = 0	0.05	-	10	ms	

Table 62. VDAC Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VDAC ACTIVE MODE – AC (CONTINUED)						
$VDAC_{OS-START}$	Start-up Overshoot • V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	-	1.0	2.0	%	
$VDAC_{LO\ TRANSIENT}$	Transient Load Response • V_{IN} = V_{INMIN}, V_{INMAX}	-	1.0	2.0	%	
$V_{DACLI\ TRANSIENT}$	Transient Line Response • IL = 75% of IL_{MAX}	-	5.0	8.0	mV	
$t_{MODE-VDAC}$	Mode Transition Time • From low power to active V_{IN} = V_{INMIN}, V_{INMAX} IL = IL_{MAXLP}	-	-	100	µs	
$VDAC_{MODE\ RES}$	Mode Transition Response • From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX} IL = IL_{MAXLP}	-	1.0	2.0	%	

7.5.6.9 VGEN1, VGEN2

General purpose LDOs, VGEN1, and VGEN2, are provided for expansion of the power tree to support peripheral devices, which could include EMMC cards, WLAN, BT, GPS, or other functional modules. These regulators include programmable set points for system flexibility. VGEN1 has an internal PMOS pass FET, and is powered from the SW5 buck for an efficiency advantage and reduced power dissipation in the pass devices. VGEN2 is powered directly from the battery.

VGEN2 has an internal PMOS pass FET, which will support loads up to 50 mA. For higher current capability, drive for an external PNP is provided. The external PNP is offered to avoid excess on-chip power dissipation at high loads and large differentials between BP and the output settings. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option. The external PNP device is always connected to the BP line in the application. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G which is capable of handling up to 250 mW of continuous dissipation at minimum footprint and 75 °C of ambient. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability, a total resistance of 60 mΩ ±20% in series with the output capacitance is required. The total resistance includes the ESR of the capacitor plus an external resistance provided by a discrete resistor or PCB circuit trace.

Table 63. VGEN1 Control Register Bit Assignments

Parameter	Value	Output Voltage	ILoad max
VGEN1[2:0]	000	1.2000	250 mA
	001	1.2500	250 mA
	010	1.3000	250 mA
	011	1.3500	250 mA
	100	1.4000	250 mA
	101	1.4500	250 mA
	110	1.5000	250 mA
	111	1.5500	250 mA

The nominal output voltage of VGEN1 is SPI configurable, and can be 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.4 V, 1.45 V, 1.5 V, or 1.55 V.

The nominal output voltage of VGEN2 is SPI configurable, and can be 2.5 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 3.15 V, or 3.3 V. The output current when working with the internal pass FET is 50 mA, and could be up to 250 mA when working with an external PNP.

Table 64. VGEN2 Control Register Bit Assignments

Parameter	Value	Output Voltage	ILoad max	
			VGEN2CONFIG=0 Internal Pass FET	VGEN2CONFIG=1 External PNP
VGEN2[2:0]	000	2.50	50 mA	250 mA
	001	2.70	50 mA	250 mA
	010	2.80	50 mA	250 mA
	011	2.90	50 mA	250 mA
	100	3.00	50 mA	250 mA
	101	3.10	50 mA	250 mA
	110	3.15	50 mA	250 mA
	111	3.30	50 mA	250 mA

Table 65. VGEN1 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
GENERAL						
V_{GEN1IN}	Operating Input Voltage Range V_{INMIN} to V_{INMAX} • All settings	1.75	1.8	1.85	V	
I_{GEN1}	• Operating Current Load Range IL_{MIN} to IL_{MAX}	0.0	-	250	mA	
VGEN1 ACTIVE MODE – DC						
V_{GEN1}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V	
$V_{GEN1LOPP}$	Load Regulation • 1.0 mA < IL < IL_{MAX} For any $V_{INMIN} < V_{IN} < V_{INMAX}$	-	0.25	-	mV/mA	
$V_{GEN1LIPP}$	Line Regulation • $V_{INMIN} < V_{IN} < V_{INMAX}$ For any $IL_{MIN} < IL < IL_{MAX}$	-	5.0	-	mV	
I_{GEN1Q}	Active Mode Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	12	-	µA	
VGEN1 LOW POWER MODE - DC						
V_{GEN1}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MINLP} < IL < IL_{MAXLP}$	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V	
I_{GEN1}	Current Load Range IL_{MINLP} to IL_{MAXLP}	0.0	-	3.0	mA	
I_{GEN1Q}	Low Power Mode Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	12	-	µA	

Table 65. VGEN1 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VGEN1 ACTIVE MODE - AC						
$VGEN1_{PSRR}$	PSRR • IL = 75% of IL_{MAX} 20 Hz to 20 kHz VGEN1[2:0] = 000-101 • IL = 75% of ILMAX 20 Hz to 20 kHz VGEN1[2:0] = 110-111	 - -	 50 45	 - -	dB	
$t_{ON-VGEN1}$	Turn-on Time • Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	-	-	1.0	ms	
$t_{OFF-VGEN1}$	Turn-off Time • Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	0.01	-	10	ms	
$VGEN1_{OS-START}$	Start-up Overshoot • V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	-	1.0	2.0	%	
$VGEN1_{LO\ TRANSIENT}$	Transient Load Response • V_{IN} = V_{INMIN}, V_{INMAX}	-	1.0	2.0	%	
$V_{GEN1LI\ TRANSIENT}$	Transient Line Response • IL = 75% of IL_{MAX}	-	5.0	8.0	mV	
$t_{MODE-VGEN1}$	Mode Transition Time • From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX} IL = IL_{MAXLP}	-	-	100	µs	
$VGEN\ 1_{MODERES}$	Mode Transition Response • From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX} IL = IL_{MAXLP}	-	1.0	2.0	%	

Table 66. VGEN2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VGEN2						
V_{GEN2IN}	Operating Input Voltage Range V_{INMIN} to V_{INMAX} • All settings, BP biased	V_{NOM} +0.25	-	4.5	V	
I_{GEN2}	Operating Current Load Range IL_{MI} to IL_{MAX} • Internal Pass FET	0.0	-	50	mA	
I_{GEN2}	Operating Current Load Range IL_{MIN} to IL_{MAX} • External PNP, Not exceeding PNP max power	0.0	-	250	mA	
V_{GEN2IN}	Extended Input Voltage Range • BP Biased, Performance may out of specification for output levels VGEN2 [2:0] = 010 to 111	UVDET	-	4.5	V	

Table 66. VGEN2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VGEN2 ACTIVE MODE - DC						
V_{GEN2}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V	
$V_{GEN2LOPP}$	Load Regulation • 1.0 mA < IL < IL_{MAX}, For any $V_{INMIN} < V_{IN} < V_{INMAX}$	-	0.20	-	mV/mA	
$V_{GEN2LIPP}$	Line Regulation • $V_{INMIN} < V_{IN} < V_{INMAX}$ For any $IL_{MIN} < IL < IL_{MAX}$	-	8.0	-	mV	
I_{GEN2Q}	Active Mode Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	30	-	µA	
VGEN2 LOW POWER MODE - DC - VGEN2MODE=1						
V_{GEN2}	Output Voltage V_{OUT} • $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MINLP} < IL < IL_{MAXLP}$	V_{NOM} - 3%	V_{NOM}	V_{NOM} + 3%	V	
I_{GEN2}	Current Load Range IL_{MINLP} to IL_{MAXLP}	0.0	-	3.0	mA	
I_{GEN2Q}	Low Power Mode Quiescent Current • $V_{INMIN} < V_{IN} < V_{INMAX}$ IL = 0	-	8.0	-	µA	
VGEN2 ACTIVE MODE - AC						
$VGEN2_{PSRR}$	PSRR - IL = 75% of ILmax, 20 Hz to 20 kHz • $V_{IN} = V_{INMIN}$ + 100 mV • $V_{IN} = V_{NOM}$ + 1.0 V	- -	40 50	- -	dB	
$t_{ON-VGEN22}$	Turn-on Time • Enable to 90% of end value $V_{IN} = V_{INMIN}$, V_{INMAX}, IL = 0	-	-	1.0	ms	
$t_{OFF-VGEN2}$	Turn-off Time • Disable to 10% of initial value $V_{IN} = V_{INMIN}$, V_{INMAX}, IL = 0	0.05	-	10	ms	
$VGEN2_{OS-START}$	Start-up Overshoot • $V_{IN} = V_{INMIN}$, V_{INMAX} IL = 0	-	1.0	2.0	%	
$VGEN2_{LO\ TRANSIENT}$	Transient Load Response • $V_{IN} = V_{INMIN}$, V_{INMAX}	-	1.0	2.0	%	
$V_{GEN2LI\ TRANSIENT}$	Transient Line Response • IL = 75% of IL_{MAX}	-	5.0	8.0	mV	
$t_{MODE-VGEN2}$	Mode Transition Time • From low power to active $V_{IN} = V_{INMIN}$, V_{INMAX}, IL = IL_{MAXLP}	-	-	100	µs	
$VGEN\ 2_{MODERES}$	Mode Transition Response • From low power to active and from active to low power $V_{IN} = V_{INMIN}$, V_{INMAX}, IL = IL_{MAXLP}	-	1.0	2.0	%	

7.6 Battery Management

BATTERY CHARGER NO LONGER SUPPORTED ON MC34708.

7.7 Analog to Digital Converter

The ADC core is a 10-bit converter. The ADC core and logic run at an internally generated frequency of approximately 1.33 MHz. The ADC is supplied from VCORE. The ADC core has an integrated auto calibration circuit which reduces the offset and gain errors.

7.7.1 Input Selector

The ADC has 16 input channels. Table 67 gives an overview of the characteristics of each of these channels.

Table 67. ADC Inputs

Channel	Signal read	Input Level	Scaling	Scaled Version
0	Battery Voltage (BATTISNSN)	0 – 4.8 V	/2	0 – 2.4 V
1	Battery Current (BATTISNSN-BATTISNSP)	-80 mV – +80 mV (62)	x15	-1.2 to +1.2 V
2	Application Supply (BPSNS)	0 to 4.8 V	/2	0 – 2.4 V
3	Die temperature	-40 – 150 °C	x1	1.2 – 2.4 V
4	Reserved	Reserved	Reserved	Reserved
5	USB Voltage (VBUS)	0 – 6.0 V	x0.4	0 – 2.4 V
6	Reserved	Reserved	Reserved	Reserved
7	Reserved	Reserved	Reserved	Reserved
8	Coincell Voltage	0 – 3.6 V	x2/3	0 – 2.4 V
9	ADIN9 (63)	0 – 2.4 V	x1	0 – 2.4 V
10	ADIN10 (63)	0 – 2.4 V	x1	0 – 2.4 V
11	ADIN11 (63)	0 – 2.4 V	x1	0 – 2.4 V
12	ADIN12/TSX1 (64)	0 – 2.4 V	x1/x2	0 – 2.4 V
13	ADIN13/TSX2 (64)	0 – 2.4 V	x1/x2	0 – 2.4 V
14	ADIN14/TSY1 (64)	0 – 2.4 V	x1/x2	0 – 2.4 V
15	ADIN15/TSY2 (64)	0 – 2.4 V	x1/x2	0 – 2.4 V

Notes
62. Equivalent to -4.0 A to +4.0 A of current with a 20 mOhm sense resistor.
63. Input must not exceed the BP voltage.
64. Input must not exceed BP or VCORE.

Some of the internal signals are first scaled to adapt the signal range to the input range of the ADC. The battery current is indirectly read out by the voltage drop over the resistor in the charge path and battery path respectively. For details on scaling, see Dedicated Readings.

Table 68. ADC Input Specification

Parameter	Condition	Min	Typ	Max	Units
Source Impedance	No bypass capacitor at input	-	-	5.0	kOhm
	Bypass capacitor at input 10 nF	-	-	30	kOhm

When exceeding the maximum input of the ADC at the scaled or unscaled inputs, the reading result will return a full scale. It has to be noted however, that this full scale does not necessarily yield a 1022 DEC reading due to the offsets and calibration applied. The same applies for when going below the minimum input where the corresponding 0000 DEC reading may not be returned.

7.7.2 Control

The ADC parameters are programmed by the processor via the SPI. When a reading sequence is finished, an interrupt ADCDONEI is generated. The interrupt can be masked with the ADCDONEM bit.

The ADC is automatically calibrated every time the PMIC is powered on.

The ADC is enabled by setting ADEN bit high. The ADC can start a series of conversions through SPI programming by setting the ADSTART bit. If the ADEN bit is low, the ADC will be disabled and in low power mode. The ADC is automatically calibrated every time PMIC is powered.

The conversions will begin after a small analog synchronization of up to 30 microseconds, plus a programmable delay from 0 (default) up to 600 μS, by programming the bits ADDLY1[3:0]. The ADDLY2[3:0] controls the delay between each of the conversions from 0 to 600 μS. ADDLY3[3:0] controls the delay after the final conversion, and is only valid when ADCONT is high. ADDLY1, 2, and 3 are set to 0 by default.

Table 69. ADDLYx[3:0]

ADDLYx[3:0]	Delay in μs
0000	0
0001	40
0010	80
0011	120
0100	160
0101	200
0110	240
0111	280
1000	320
1001	360
1010	400
1011	440
1100	480
1101	520
1110	560
1111	600

A maximum of 8 conversions will take place when the ADC is started. The register ADSELx[3:0] selects the channel which the ADC will read and store in the ADRESULTx register. The ADC will always start at the channel indicated in ADSEL0, and read up to and including the channel set by the ADSTOP[2:0] bits. For example, when ADSTOP[2:0] = 010, it will request the ADC to read channels indicated in ADSEL0, ADSEL1, and ADSEL2. When ADSTOP[2:0] = 111, all eight channels programmed by the value in ADSEL0-7 will be read. When the ADCONT bit is set high, it allows the ADC to continuously loop and read the channels

from address 0 to the stop address programmed in ADSTOP. By default, the ADCONT is set low (disabled). In the continuous mode, the ADHOLD bit will allow the software to hold the ADC sequencer from updating the results register while the ADC results are read. Once the sequence of A/D conversions is complete, the ADRESULTx results are stored in 4 SPI registers (ADC 4 - ADC 7).

7.7.3 Dedicated Readings

7.7.3.1 Channel 0 Battery Voltage

The battery voltage is read at the BATTISNSN pin on channel 0. The battery voltage is first scaled as V(BATT)/2 to fit the input range of the ADC.

Table 70. Battery Voltage Reading Coding

Conversion Code ADRESULTx[9:0]	Voltage at Input ADC in V	Voltage at BATTISNSN in V
1 111 111 111	2.400	4.800
1 000 010 100	1.250	2.500
0 000 000 000	0.000	0.000

7.7.3.2 Channel 1 Battery Current (Optional)

Battery current is only valid after a battery voltage reading. The current flowing into and out of the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATTISNSN and BATTISNSP.

The voltage difference between BATTISNSN and BATTISNSP is amplified to fit the ADC input range as V(BATTISNSP - BATTISNSN)*15. Since battery current can flow in both directions, the conversion is read out in 2's complement. Positive readings correspond to the current flowing into the battery, and negative readings to the current flowing out of the battery.

Table 71. Battery Current Reading Coding

Conversion Code ADRESULTx [9:0]	Voltage at input ADC in mV	BATTISNSN–BATTISNSP in mV	Current through 20 mOhm in mA	Current Flow
0 111 111 111	1200.00	80	4000	To battery
0 000 000 001	2.346	0.156	7.813	To battery
0 000 000 000	0	0	0	-
1 111 111 111	-2.346	-0.156	7.813	From battery
1 000 000 000	-1200.00	-80	4000	From battery

The value of the sense resistor used determines the accuracy of the result, as well as the available conversion range. Note that excessively high values can impact the operating life of the device due to extra voltage drop across the sense resistor.

If battery current sense is required, add a 20 mΩ resistor between the BATTISNSN and BATTISNSP terminal, as shown in Figure 19.

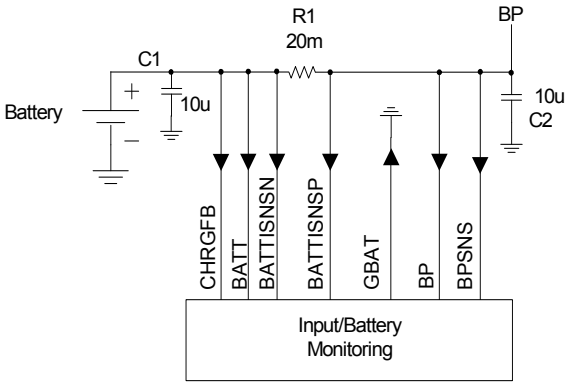


Figure 19. Input Configuration with Battery Current Sense

7.7.3.3 Channel 2 Application Supply

The application supply voltage is read at the BPSNS pin on channel 2. The battery voltage is first scaled as V_{BPSNS} /2 to fit the input range of the ADC.

Table 72. Application Supply Voltage Reading Coding

Conversion Code ADRESULTx[9:0]	Voltage at Input ADC in V	Voltage at BPSNS in V
1 111 111 111	2.400	4.800
1 000 010 101	1.250	2.500
0 000 000 000	0.000	0.000

7.7.3.4 Channel 3 Die Temperature

The relation between the read out code and temperature is given in Table 73.

Table 73. Die Temperature Voltage Reading

Parameter	Min	Typ	Max	Unit
Die Temperature Read Out Code at 25 °C	-	680	-	Decimal
Slope temperature change per LSB	-	+0.426	-	°C/LSB
Slope error	-	-	5.0	%

The Actual Die Temperature is obtained as follows: Die Temp = 25 + 0.426 * (ADC Code - 680)

7.7.3.5 Channel 4 Reserved

Channel 4 is reserved.

7.7.3.6 Channel 5 VBUS Voltage

The VBUS voltage is measured at the VBUS pin on channel 5. The VBUS voltage is first scaled in order to fit the input range of the ADC by multiplying by 0.4.

7.7.3.7 Channel 6 and 7 Reserved

Channel 6 is reserved.

7.7.3.8 Channel 8 Coin Cell Voltage

The voltage of the coin cell connected to the LICELL pin can be read on channel 8. Since the voltage range of the coin cell exceeds the input voltage range of the ADC, the LICELL voltage is scaled as V(LICELL)*2/3. See .

Table 74. Coin Cell Voltage Reading Coding

Conversion Code ADRESULTx[9:0]	Voltage at ADC input (V)	Voltage at LICELL (V)
1 111 111 110	2.400	3.6
1 000 000 000	1.200	1.8
0 000 000 000	0.000	0

7.7.3.9 Channel 9-11 ADIN9-ADIN11

There are 3 general purpose analog input channels that can be measured through the ADIN9-ADIN11 pins.

7.7.3.10 Channel 12-15 ADIN12-ADIN15

If the touch screen is not used, the inputs TSX1, TSX2, TSY1, and TSY2 can be used as general purpose inputs. They are respectively mapped on ADC channels 12, 13, 14, and 15.

7.7.4 Touch Screen Interface

The touch screen interface provides all circuitry required for the readout of a 4-wire resistive touch screen. The touch screen X plate is connected to TSX1 and TSX2, while the Y plate is connected to TSY1 and TSY2. A local supply TSREF will serve as a reference. Several readout possibilities are offered.

If the touchscreen is not used, the inputs TSX1, TSX2, TSY1, and TSY2 can be used as general purpose inputs. They are respectively mapped on ADC channels 12, 13, 14, and 15.

Touch Screen Pen detection bias can be enabled via the TSPENDETEN bit in the AD0 register. When this bit is enabled and a pen touch is detected, the TSPENDET bit in the Interrupt Status 0 register is set and the INT pin is asserted - unless the interrupt is masked. Pen detection is only active when TSEN is low.

The reference for the touch screen (Touch Bias) is TSREF and is powered from VCORE. During touch screen operation, TSREF is a dedicated regulator. No loads other than the touch screen should be connected here. When the ADC performs non touch screen conversions, the ADC does not rely on TSREF and the reference is disabled.

The readouts are designed such that the on chip switch resistances are of no influence on the overall readout. The readout scheme does not account for contact resistances, as present in the touch screen connectors. The touch screen readings will have to be calibrated by the user or the factory, where one has to point with a stylus to the opposite corners of the screen. When reading the X-coordinate, the 10-bit ADC reading represents a 10-bit coordinate, with ‘0’ for a coordinate equal to X-, and full scale ‘1023’ when equal to X+. When reading the Y-coordinate, the 10-bit ADC reading represents a 10-bit coordinate, with ‘0’ for a coordinate equal to Y-, and full scale ‘1023’ when equal to Y+. When reading contact resistance, the 10-bit ADC reading represents the voltage drop over the contact resistance created by the known current source, multiplied by 2.

The X-coordinate is determined by applying TSREF over the TSX1 and TSX2 pins, while performing a high-impedance reading on the Y-plate through TSY1. The Y-coordinate is determined by applying TSREF between TSY1 and TSY2, while reading the TSX1 pin. The contact resistance is measured by applying a known current into the TSY1 pin of the touch screen and through the TSX2 pin, which is grounded. The voltage difference between the two remaining terminals TSY2 and TSX1 is measured by the ADC, and equals the voltage across the contact resistance. Measuring the contact resistance helps determine if the touch screen is touched with a finger or a stylus.

The TSSELx[1:0] allows the application processor to select its own reading sequence. The TSSELx[1:0] determines what is read during the touch screen reading sequence, as shown in Table 75. The Touchscreen will always start at TSSEL0 and read up to and including the channel set by TSSEL at the TSSTOP[2:0] bits. For example when TSSTOP[2:0] = 010, it will request the ADC to read channels indicated in TSSEL0, TSSEL1, and TSSEL2. When TSSTOP[2:0] = 111, all eight addresses will be read.

Table 75. Touch Screen Action Select

TSSELx[1:0]	Signals Sampled
00	Dummy to discharge TSREF cap
01	X plate
10	Y –plate
11	Contact

The touch screen readings can be repeated, as in the following example readout sequence, to reduce the interrupt rate and to allow for easier noise rejection. The dummy conversion inserted between the different readings allows the references in the system to be pre-biased for the change in touch screen plate polarity. It will read out as ‘0’.

A touchscreen reading will take precedence over an ADC sequence. If an ADC reading is triggered during a touchscreen event, the ADC sequence will be overwritten by the Touchscreen data.

The first Touch screen conversion can be delayed from 0 (default) to 600 μs by programming the TSDLY1[3:0] bits. The TSDLY2[3:0] controls the delay between each of the touch screen conversions from 0 to 600 μs. TSDLY[2:0] sets the delay after the last address is converted. TSDLY1, 2, and 3 are set to 0 by default.

Table 76. TSDLYx[3:0]

TSDLYx[3:0]	Delay in uS
0000	0
0001	40
0010	80
0011	120
0100	160
0101	200
0110	240
0111	280
1000	320
1001	360
1010	400
1011	440
1100	480
1101	520
1110	560
1111	600

To perform a touch screen reading, the processor must do the following:

- Enable the touch screen with TSEN
- Select the touch screen sequence by programming the TSSEL0-TSSEL7 SPI bits.
- Program the TSSTOP[2:0]
- Program the delay between the conversion via the TSDLY1 and TSDLY2 settings.
- Trigger the ADC via the TSSTART SPI bit
- Wait for an interrupt indicating the conversion is done TSDONEI
- And then read out the data in the ADRESULTx registers

7.7.5 ADC Specifications

Table 77. ADC Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
ADC						
I_{CONVER}	Conversion Current	-	1.0	-	mA	
V_{ADCIN}	Converter Core Input Range • Single ended voltage readings • Differential readings	 0.0 -1.2	 - -	 2.4 1.2	V	
$t_{CONVERT}$	Conversion Time per channel	-	-	10	µs	
	Integral Non-linearity	-	-	3	LSB	
	Differential Non-linearity	-	-	1	LSB	
	Zero Scale Error (Offset)	-	-	5	LSB	
	Full Scale Error (Gain)	-	-	10	LSB	
	Drift over temperature	-	-	10	LSB	
$t_{ON-OFF-ADC}$	Turn on/off time	-	-	31	µs	
BATTERY CURRENT READING[65]						
	Amplifier Gain	19	20	21		
	Amplifier Offset	-2.0	-	2.0	mV	
	Sense Resistor	-	20	-	mΩ	
DIE TEMPERATURE VOLTAGE READING						
	Die Temperature Read Out Code at 25 °C	-	680	-	Decimal	
	Slope temperature change per LSB	-	0.426	-	°C/LSB	
	Slope error	-	-	5.0	%	

Notes

65. Amplifier Bias Current accounted for in overall ADC current drain

7.8 Auxiliary Circuits

7.8.1 General Purpose I/Os

The MC34708 contains four configurable GPIOs for general purpose use. When configured as outputs, they can be configured as open-drain (OD) or CMOS (push-pull outputs). These GPIOs are low voltage capable (1.2 or 1.8 V). In open drain configuration these outputs can only be pulled up to 2.5 V maximum.

Each individual GPIO has a dedicated 16-bit control register. Table 78 provides detailed bit descriptions.

Table 78. GPIOLVx Control

SPI Bit	Description
DIR	GPIOLVx direction 0: Input (default) 1: Output
DIN	Input state of the GPIOLVx pin 0: Input low 1: Input High
DOUT	Output state of GPIOLVx pin 0: Output Low 1: Output High
HYS	Hysteresis 0: CMOS in 1: Hysteresis (default)
DBNC[1:0]	GPIOLVx input debounce time 00: no debounce (default) 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce
INT[1:0]	GPIOLVx interrupt control 00: None (default) 01: Falling edge 10: Rising edge 11: Both edges
PKE	Pad keep enable 0: Off (default) 1: On
ODE	Open drain enable 0: CMOS (default) 1: OD
DSE	Drive strength enable 0: 4.0 mA (default) 1: 8.0 mA
PUE	Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default)

Table 78. GPIOLVx Control

SPI Bit	Description
PUS[1:0]	Pull-up/Pull-down enable 00: 10 K active pull-down 01: 10 K active pull-up 10: 100 K active pull-down 11: 100 K active pull-up (default)
SRE[1:0]	Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast
x= 0, 1, 2, or 3	

7.8.2 PWM Outputs

There are two PWM outputs on the MC34708. PWM1 and PWM2 are controlled by the PWMxDUTY and PWMxCLKDIV registers shown in Table 79.The base clock will be the 2.0 MHz divided by 32.

Table 79. PWMx Duty Cycle Programming

PWMxDC[5:0]((66))	Duty Cycle
000000	0/32, Off (default)
000001	1/32
…	…
010000	16/32
…	…
011111	31/32
1xxxxx	32/32, Continuously On

Notes
66. “x” represent 1 and 2

32.768 kHz Crystal Oscillator RTC Block Description and Application Information

Table 80. PWMx Clock Divider Programming

PWMxCLKDIV[5:0]((67))	Duty Cycle
000000	Base Clock
000001	Base Clock / 2
…	…
001111	Base Clock / 16
…	…
111111	Base Clock / 64

Notes
67. “x” represent 1 and 2

7.8.3 General Purpose LED Drivers

To turn on the LEDs, the following bits must be set, CHRLEDxEN = 1, CHRGLEDOVRD =1, THERM bit = 1, and programming the duty cycle > 0/32.

Table 81. LED Driver Control

THERM	CHRGLEDxEN[68]	CHRGLEDOVRD	CHRGLEDx[68]
x	0 (default)	0	Off
1	x	x	Off
0	1	1	On
	0	1	Off

Notes
68. “x” represents R or G

The general purpose LED drivers, CHRGLEDR, and CHRLEDG are independent current sink channels. Each driver channel features programmable current levels via CHRGLEDx[1:0], as well as programmable PWM duty cycle settings with CHRGLEDxDC[5:0]. By a combination of level and PWM settings, each channel provides flexible LED intensity control.

Table 82. General Purpose LED Drivers Current Programming

CHRGLEDx[1:0]	CHRGLEDx Current Level (mA)
00	3.5
01	7.0 (default)
10	10
11	12
“x” represents for R, and G	

Table 83. General Purpose LED Drivers Duty Cycle Programming

CHRGLEDxDC[5:0]	Duty Cycle
000000	0/32, Off
000001	1/32
…	…
010000	16/32
…	…
011111	31/32
1xxxxx	32/32, Continuously On
“x” represents R, and G	

The general purpose LED drivers include ramp up and ramp down patterns implemented in hardware. Ramping is enabled for each of the drivers using the corresponding CHRGLEDxRAMP bits, only when the repetition rate is 256 Hz.

The ramp itself is generated by increasing or decreasing the PWM duty cycle with a 1/32 step every 1/64 seconds. The ramp time is therefore a function of the initial set PWM cycle and the final PWM cycle. As an example, starting from 0/32 and going to 32/32 will take 500 ms, while going to from 8/32 to 16/32 takes 125 ms.

Note that the ramp function is executed upon every change in PWM cycle setting. If a PWM change is programmed via the SPI when CHRGLEDxRAMP = 0, the change is immediate rather than spread out over a PWM sweep.

In addition, programmable blink rates are provided. Blinking is obtained by lowering the PWM repetition rate of each of the drivers through CHRGLEDxPER[1:0], while the on period is determined by the duty cycle setting. To avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened.

Table 84. General Purpose LED Drivers Period Control

CHRGLEDxPER[1:0]	Repetition Rate	Units
00	256	Hz
01	8.0	Hz
10	1.0	Hz
11	1/2	Hz

Table 85. LED Driver Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
General Purpose LED Driver						
	Absolute Accuracy	-	-	30	%	
	Matching - At 1.0 V, 12 mA	-	-	4.0	%	
	Leakage - CHRGLEDxDC [5:0]=000000	-	-	1.0	μA	

7.8.4 Mini/Micro USB Switch

The MC34708 is able to multiplex the 5 pins to support UART and high-speed USB2.0 data communications, a mono/stereo-audio/microphone headset, or other accessories. To identify what accessory is plugged into the Mini or Micro-USB connector, the MC34708 supports various detection mechanisms, including the VBUS detection and ID detection. A highly accurate 5-bit ADC is offered to distinguish the 32 levels of ID resistance, and to identify the button pressed in a cord remote control, while an Audio Type 1 cable is attached. After identifying the accessory attached, the MC34708 configures itself to support the accessory and interrupts a host via the INT pin. The processor can evaluate what caused the interrupt via the SPI/I^2C bus. The MC34708 is also able to identify some non-supported accessories, such as video cables, phone-powered devices, etc.

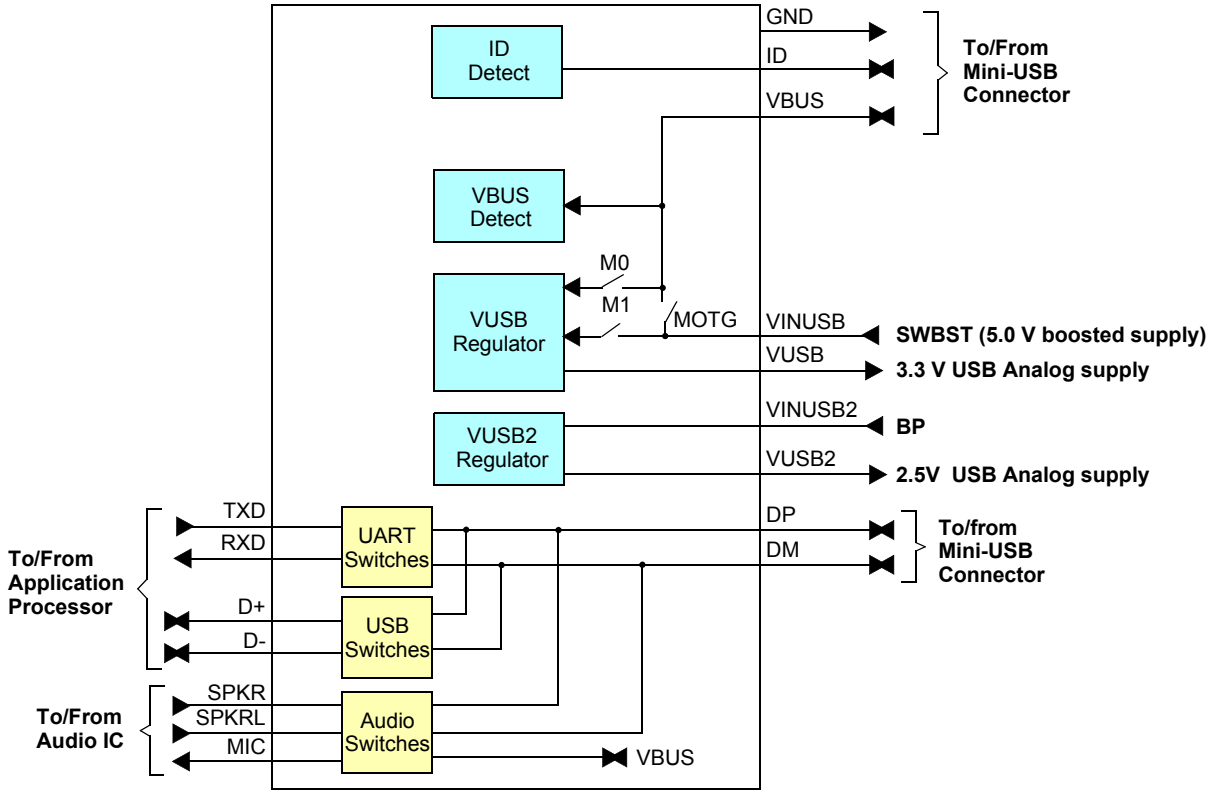


Figure 20. USB Interface

7.8.4.1 Supplies

The MC34708 provides the regulators required to power the PHY in the i.MX50, i.MX51, and i.MX53 processors, which are VUSB2 (detailed Linear Regulators (LDOs)), and VUSB. The IC also provides the 5.0 V supply for USB OTG operation.

The VUSB regulator is used to supply 3.3 V to the external USB PHY. The input to the VUSB regulator can be supplied from the VBUS wire of the cable when supplied by a host (PC or Hub), or by the SWBST voltage via the VINUSB pin. The VUSB regulator is powered from the SWBST boost supply to ensure OTG current sourcing compliance through the normal discharge range of the main battery. The VUSBSEL SPI bit is used to make the selection between a host or OTG mode operation.

Table 86. VUSB Input Source Control (69)

Parameter	Value	Function
V_{USBSEL}	0	Powered by Host: VBUS powers VUSB regulator (switch M0 closed and M1 open)
	1	OTG mode: SWBST internally switched to supply the VUSB regulator (switch M1 closed, M0 open), and SWBST will drive VBUS from the VINUSB pin as long as SPI bit OTGEN is set = 1.

Notes

69. VUSBSEL = 1 and OTGEN = 1 only close the switch between the VINUSB and VBUS pins, but do not enable the SWBST boost regulator (which should be enabled with SWBSTEN = 1)

The VUSB regulator defaults to ON when PUMS4:1 = [0100], and is supplied by the SWBST output. As shown in Figure 20, this means the M0 and MOTG switches are open, while the M1 switch is closed.

When PUMS4:1 is not equal to [0100], the VUSB regulator can not be enabled unless 5.0 V is present on the VBUS pin. If VBUS is detected during a cold start, then the VUSB regulator will be enabled and powered ON in the sequence shown in Startup Requirements, and it will default to be supplied by the VBUS pin. This means switch M0 is closed and switch M1 and MOTG in Figure 20 are open. If VBUS is not detected at cold start, then the VUSB regulator cannot be enabled. If VBUS is detected later, the VUSB regulator will be enabled automatically and supplied from the VBUS pin. The VUSBEN SPI bit is initialized at startup, based on the PUMS4:1 configuration. With PUMS4:1 not equal to [0100], the VUSBEN SPI bit will default to a 1 on power up and

will reset to a 1, when either RESETB is valid or VBUS is invalid. This allows the VUSBEN regulator to be enabled automatically if the VUSB regulator was disabled by software. With PUMS4:1 equal to [0100], the VUSBEN bit will be enabled in the power up sequence.

The MC34708 also supports USB OTG mode by supplying 5.0 V to the VBUS pin. The OTGEN SPI bit along with the VUSBSEL SPI bit, control switching the SWBST to drive VBUS in OTG mode. When OTGEN = 1 and VUSBSEL = 1, SWBST will be driving the VBUS (switch M1 and MOTG are closed, and the M0 switch is open). When OTG mode is disabled, the switch (MOTG) from VINUSB to VBUS will be open.

In OTG mode, the VUSB regulator is enabled by setting the VUSBEN SPI bit to a 1. When SWBST is supplying the VBUS pin (OTG Mode), it will generate a USBDET interrupt. The USBDET interrupt while in OTG mode should not be interpreted as being powered by the host by software.

Table 87. VUSB/OTG Switch Configuration

Mode	OTGEN	VUSBSEL	Switches Enabled (Closed)	Switches Disabled (Open)
VUSB powered from VBUS pin	0	0	M0	M1, MOTG
VUSB powered from VINUSB pin	0	1	M1	M0, MOTG
Invalid option	1	0	-	-
OTG Mode (VUSB powered from VINUSB pin and SWBST	1	1	M1, MOTG	M0

Table 88. VUSB Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
VUSB REGULATOR						
V_{USBIN}	Operating Input Voltage Range V_{INMIN} to V_{INMAX} • Supplied by VBUS • Supplied by SWBST	 4.4 -	 5.0 -	 5.25 5.75	V	
I_{USB}	Operating Current Load Range IL_{MIN} to IL_{MAX}	0.0	-	100	mA	
VUSB ACTIVE MODE - DC						
V_{USB}	Output Voltage V_{OUT} • V_{INMIN} < V_{IN} < V_{INMAX} IL_{MIN} < IL < IL_{MA}	V_{NOM} - 4%	3.3	V_{NOM} + 4%	V	
$V_{USBLOPP}$	Load Regulation • 0 < IL < IL_{MAX} from DM / DP, For any V_{INMIN} < V_{IN} < V_{INMAX}	-	1.0	-	mV/mA	
$V_{USBLIPP}$	Line Regulation • V_{INMIN} < V_{IN} < V_{INMAX}, For any IL_{MIN} < IL < IL_{MAX}	-	-	20	mV	
$t_{OFF-VUSB}$	Turn-off Time • Disable to 0.8 V, per USB OTG specification parameter VA_SESS_VLD V_{IN} = V_{INMIN}, V_{INMAX} IL = 0	-	-	1.3	sec	
VUSB ACTIVE MODE - AC						
$VUSB_{PSRR}$	PSRR - IL = 75% of IL_{MAX} 20 Hz to 20 kHz • V_{IN} = V_{INMIN} + 100 mV	-	65	-	dB	

7.8.4.2 Accessory Identification

The MC34708 monitors both the ID pin and the VBUS pin. When an accessory attachment is detected, the accessory identification state machine will enter Active mode to start the identification flow. The ID detection state machine will determine

what ID resistor is attached and the Power Supply Type Identification or PSTI circuit will determine what type of power supply is connected. The 32 kHz crystal must be placed across the XTAL 1 and XTAL2 pins for the accessory identification to work.

An identification conclusion is made when the identification flow is finished. The corresponding bit in the USB Device Type/Status register is set to indicate the device type, and the ATTACH bit in the USB Interrupt Status register is set to inform the baseband. If the attached accessory can't be identified, the Unknown_Atta bit in the USB Interrupt Status register is set.

The MC34708 will automatically detect three types of accessories.

1. Recognized and supported. The following accessories are identified and configured automatically: USB port, UART, Audio Type 1 cable, TTY accessory, USB jig cables, and UART jig cables.
2. Recognized but not supported. The following accessories can be identified but are not supported by the MC34708 PMIC: A/V cables, Phone-Powered Devices, Audio Type 2 cables, dedicated charger, USB charger, A/V charger, 5-wire type 1 and type 2 chargers. The PMIC will detect that a charger is attached, when the VBUS voltage transitions above the setpoint, which is defaulted to 4.35 V. When above this threshold for longer than the debounce period (VBUSDB[1:0]), the USBDET interrupt is generated and USBDETS is set to a one. When the VBUS input falls below the VBUSTL[2:0] threshold, the USBDET interrupt is generated immediately without any debounce and the USBDETS bit is low. See Table 89 and Table 90. The USBOVP interrupt will be triggered when an over-voltage on VBUS (>6.5 V typical) is detected during a device attach. The over-voltage interrupt is debounce by SUP_OVP_DB[1:0] bits on Table 91.

Table 89. VBUS Debounce Times

VBUSDB[1:0]	Debounce Time (ms)
00	0
01	10
10	20
11	30

Table 90. VBUS High/low Detection Threshold

VBUSTH[2:0]	Voltage	VBUSTL[2:0]	Voltage
000	4.05	000	3.55
001	4.15	001	3.65
010	4.25	010	3.75
011	4.35 (default)	011	3.85 (default)
100	4.45	100	3.95
101	4.55	101	4.05
110	4.65	110	4.15
111	4.75	111	4.25

Table 91. Over-voltage Debounce Time SUP_OVP_DB[1:0]

SUP_OVP_DB[1:0]	Debounce Time
00	0 (default 1.0)
01	2 RTC clock cycles
10	4 RTC clock cycles
11	8 RTC clock cycles (default 2.0)

3. Not recognized accessories. All accessories that are not recognized are identified as unknown accessories.

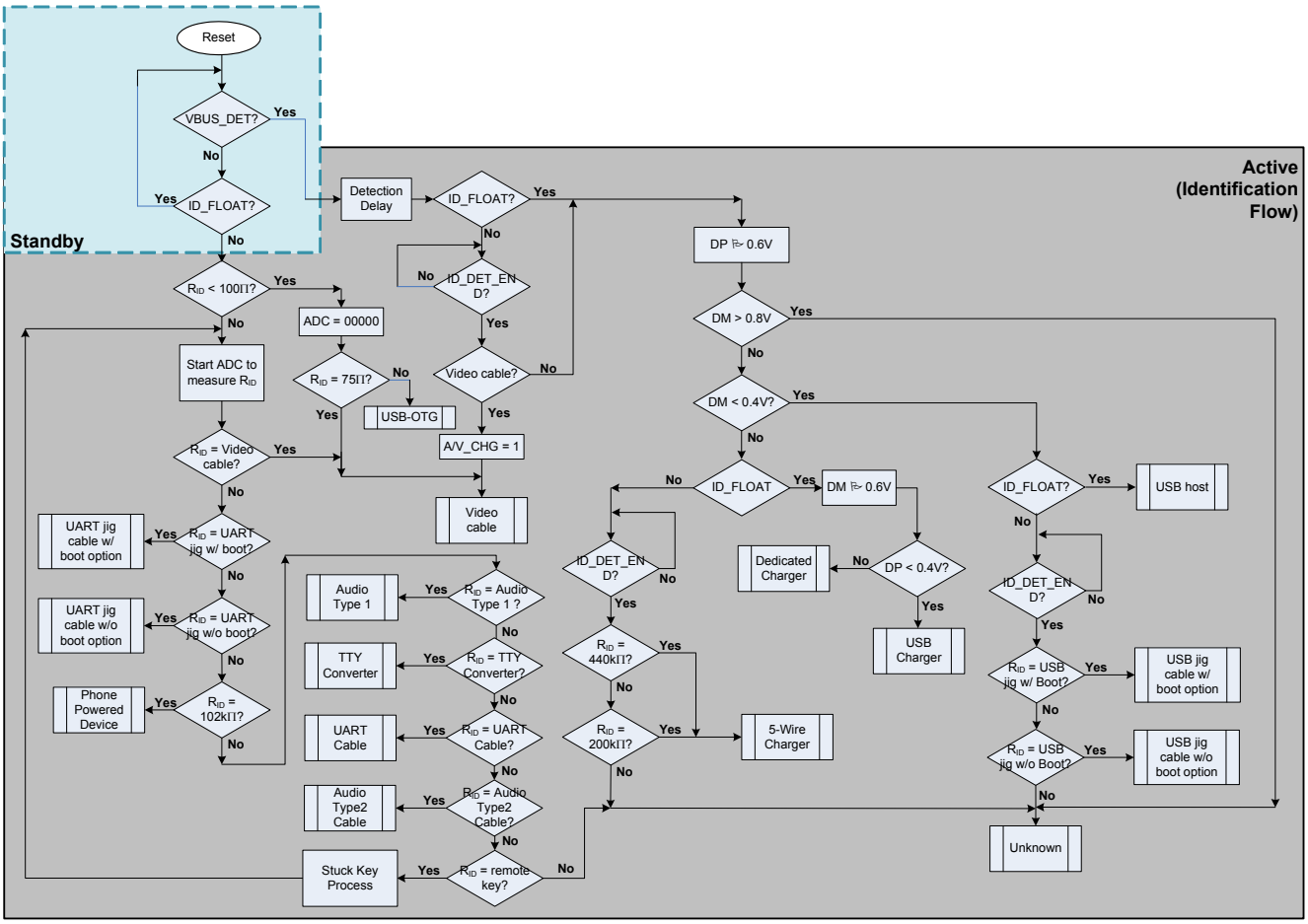


Figure 21. Identification Flow State Diagram

7.8.4.3 Id Identification

A comparator monitors the ID pin impedance to ground. When a resistor less than 1.0 MΩ is connected between the ID line and the ground, the ID_FLOATS bit in the Interrupt Sense 0 register will be set to 0. When the resistor is removed, the ID_FLOATS bit will be set to 1. A falling edge of this bit starts the identification flow, and a rising edge starts the detachment detection flow. The ID_DET_END signal is used to indicate the end of the identification.

After the ID_FLOATS bit is set to 0, the identification flow is started, and an ADC_EN signal is set to enable an ADC conversion. A 5-bit ID ADC is used to measure the ID resistance. The ADC is also used to identify what button is pressed in a cord remote control when the attached accessory is an Audio Type 1 cable.

When the conversion completes, an ADC_STATUS bit is set and the ADC result value is sent to the ADC Manual SW/Result register. The ADC_EN signal is cleared automatically after the conversion finishes.

If the ID resistance is below 2.0 kΩ, the ADC Result is set to 00000. If the ID line is floating, the ADC Result is set to 11111.

7.8.4.4 Stuck Key Identification

When the ADC conversion is finished and the ADC result is found to be a value corresponding to a remote control key of Audio Type 1 cable, a stuck key process flow will be initiated to determine whether a remote control key is stuck and to inform the baseband of the stuck key status.

Figure 22 shows the stuck key process flow. If the stuck key is detected to be released within 1.5 s, the flow will return to re-start the ID identification flow. Otherwise, a Stuck_Key Interrupt is set. When the key is released, a Stuck_Key_RCV Interrupt is generated, and the identification flow is re-started to determine the ID resistance of the attached cable.

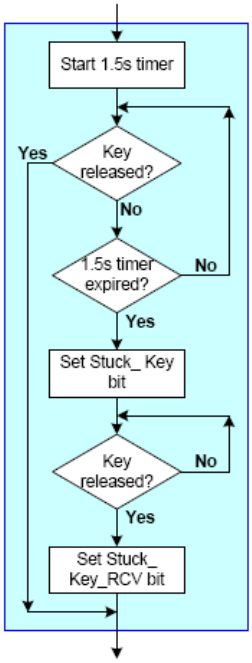


Figure 22. Stuck Key Process Flow Diagram

7.8.4.5 Power Supply Type Identification

The PSTI (Power Supply Type Identification) circuit is used in Active mode to identify the type of the connected power supply. The PSTI circuit first detects whether the DP and DM pins are shorted. If the DP and DM pins are found to be shorted, the PSTI circuit will continue to determine whether DP and DM pins are a forward short or reverse short. The detection result, together with the ID detection result, is used to determine what powered accessory is connected.

The PSTI circuit is shown in Figure 23. Its operation is described as follows.

When the MC34708 detects the VBUS_DET bit is set, the PSTI identification flow starts.

1. Wait for a Detection Delay t_D (programmable in the USB Time Delay register).
2. During t_D, check to see whether ID_FLOAT = 0. If yes, then wait for the ID_DET_END to be set and check whether the attached accessory is an A/V cable.
3. If the result is an A/V cable, set the A/V_CHG and ATTACH interrupt bits, as well as the A/V bit in USB Device Type/Status register, to inform the baseband and finish the identification flow. If not, go to step 4.
4. Enable the PSTI (PSTI_EN set to '1') at t1. When PSTI_EN rises, the SW1 switch is turned on to drive the VDAT_SRC data source voltage to DP line. In the meantime, the SW2 switch is turned on so the IDAT_SINK current source sinks a current from the DM line. At t2, the PSTI starts to compare the DM line voltage with references VDAT_REF and VCR_REF. If the DM line voltage stays above VDAT_REF, but below VCR_REF for 20 ms continuously before t4, which means the DP and DM pins are shorted, the DP/DM_short signal is set to '1' at t3. Go to step 5. If the DP and DM are not shorted, the VBUS detection completes at t4 and the VBUS_DET_END is set to '1'. The state machine will go to step 6 to determine the type of accessory, based on the DM voltage.
5. The state machine checks if the ID pin is floating. If the ID pin is not floating at t3, the PSTI circuit turns off SW1 and SW2, and the VBUS detection completes. The VBUS_DET_END is set to '1' and the state machine goes to step 6. If the ID pin is floating at t3, the PSTI circuit turns off SW1 and SW2, and then turns on SW3 and SW4 to force VDAT_SRC to the DM pin. If the DP pin is between the two thresholds VDAT_REF and VCR_REF for 20 ms continuously before t6, it means the DP and DM pins are a reverse short.The DP/DM_reverse_short is set to '1' at t5, the SW3 and SW4 are turned off, VBUS_DET_END is set to '1', and the state machine goes to step 6. If DP and DM are not a reverse short, the VBUS detection completes at t6, SW3 and SW4 are turned off, the VBUS_DET_END is set to '1', and the state machine goes to step 6.
6. The state machine decides on the attached accessory, based on the ID identification, and the VBUS identification results.

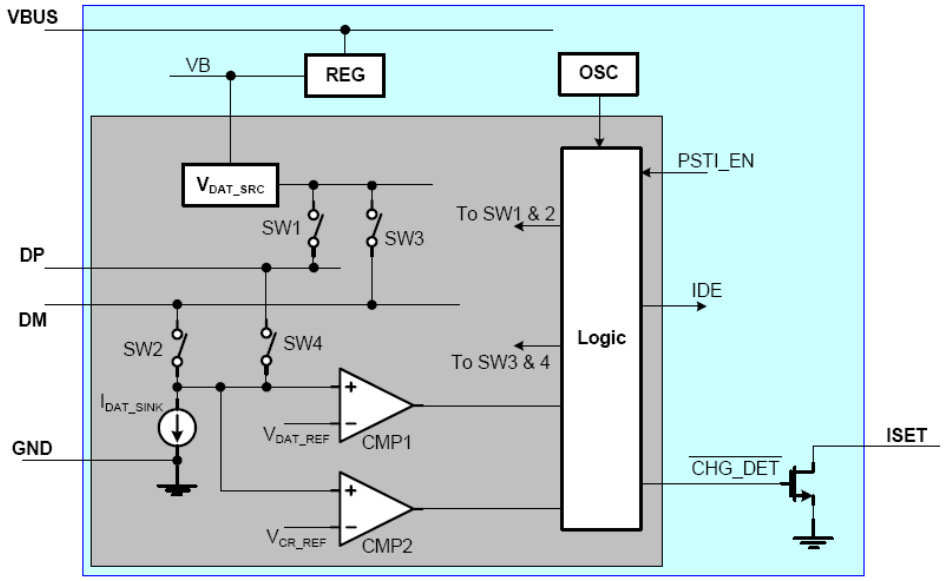


Figure 23. Power Supply Type Identification Circuit Block Diagram

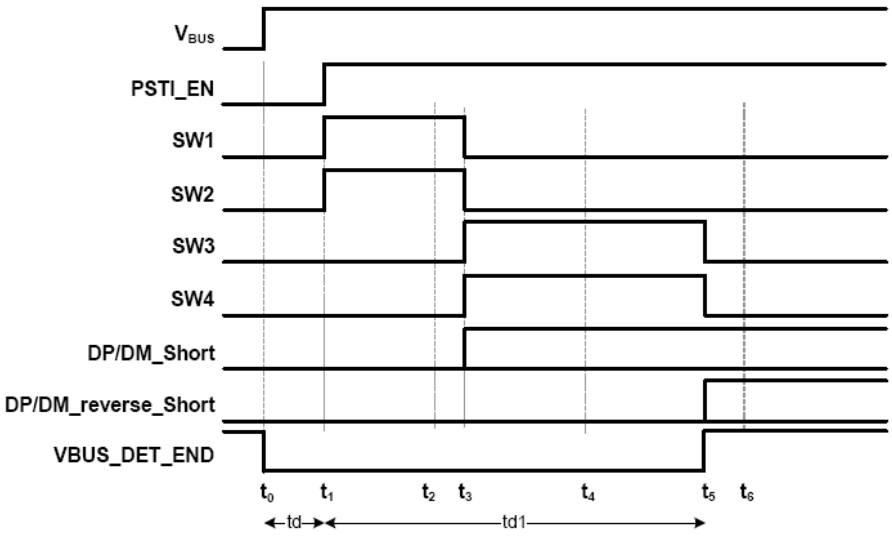


Figure 24. Operating Waveforms for the PSTI Circuit

Table 92. Timing Delays for PSTI Circuit

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

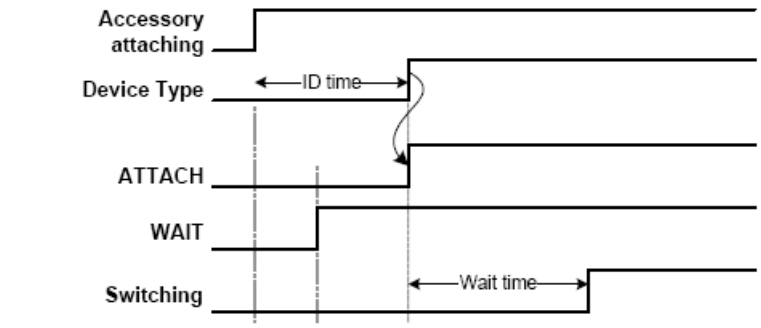
Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Switching Delay						
t_D	t1 - t0 (t_D in Default Value is TD = 0100)				ms	
	• TD = 0000	-	100	-		
	• TD = 0001	-	200	-		
	• TD = 0010	-	300	-		
	• TD = 0011	-	400	-		
	• TD = 0100	-	500	-		
	• ...	...	...	...		
	• TD = 1111	-	1600	-		
t_{SW}	t2 - t1	20	-	-	ms	
t_{SW}	t3 - t2	20	-	-	ms	
t_{SW}	t4 - t1	100	-	-	ms	
t_{SW}	t6 - t3	100	-	-	ms	

The MC34708 contains registers which hold control and status information. The register map and the description of each register can be found in the SPI/I2C Register Map section. The details of some important control bits are described as follows.

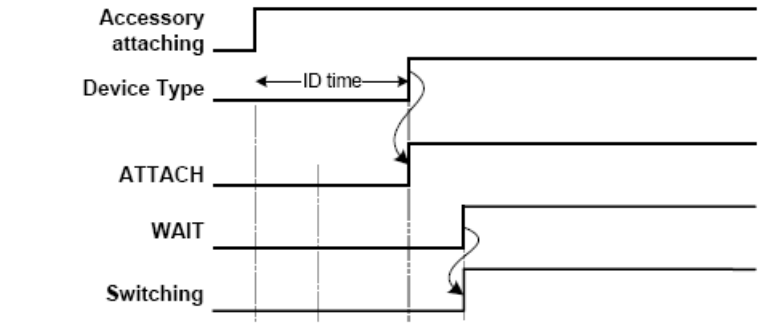
7.8.4.6 Control Functions

7.8.4.6.1 Timing of the Switching Action (WAIT BIT)

If the WAIT bit is '1' when the Attach interrupt bit is set, the MC34708 waits for a WAIT time before turning on the switches. The WAIT time is programmed by the Switching Wait bits in the Timing Set 2 register. If the WAIT bit is '0' when the Attach interrupt is generated, then the MC34708 will not turn on the switches until the WAIT bit is set to '1' by the SPI. Both cases are shown in Figure 25.



(A). WAIT = 1 when the ATTACH interrupt is generated. (VDDIO is high and INT_MASK = 1.)



(B). WAIT = 0 when the ATTACH interrupt is generated. (VDDIO is high and INT_MASK = 1.)

Figure 25. Operating Waveforms of the Wait Bit

7.8.4.6.2 Automatic Switching OR Manual Switching (Switch_open & Manual S/W Bits)

When a supported accessory is identified, the default behavior of the MC34708 automatically turns on the corresponding signal switches. The user can also choose to turn on optional signal switches manually. Switch turn on is controlled by the Manual S/W bit and the Switch_Open bits in the USB Manual SW/Result and USB Control/Device mode registers respectively.

If the Switch_Open bit is '0', the audio, UART, and USB switches are off.

If Manual S/W = 1, which is its reset value, the switches to be turned on and the outputs of the JIG and BOOT pins are determined automatically by the Device Mode register, which is the identification result. If Manual S/W = 0, the switches to be turned on are determined by the values of the USB Manual SW/Result register. The relationship between the values of the USB Manual SW/Result register and the switches to be turned on is found in SPI/I2C Register Map section.

The values of the Switch_Open and Manual S/W bits will not affect the identification flow and the timing of the signal switching action of the MC34708. The difference between Manual S/W = 1 and Manual S/W = 0 is what switches are turned on. In both cases, no switches are turned on in Standby mode. If the Manual S/W bit is changed from '1' to '0' while an accessory is attached, the already automatically turned on switches will be turned off, and the switches selected manually will be turned on. However, writing the Manual S/W bit back to '1' in Active mode will not change the switches and outputs status. Setting the Switch_Open = 1, sets the switches according to the Manual S/W bit.

Raw Data (Raw Data Bit)

The RAW DATA bit functions only when the accessory is Audio Type 1, which supports the remote control key. The RAW DATA bit determines whether to report the ID pin resistance change to the baseband when any key is pressed. When RAW DATA = 1, the ADC is enabled only when an ID line event is detected, such as when a key is pressed. In this case, the interrupt bits KP, LKP, or LKR, and the corresponding button bits in Button 1 and Button 2 registers, will be set accordingly. Detailed behavior information when RAW DATA = 1 can be found in Audio Type 1 Operation Mode.

Audio Device Type 1 - Audio with or without the Remote Control. When RAW DATA = 0, the ADC is enabled periodically to calculate the ID line resistance. Any change of ADC Result will set the ADC_Change interrupt bit to inform the baseband. The baseband can read the ADC result via the SPI. The KP, LKP, or LKR, and the button bits, will not set when RAW DATA = 0. The period of ADC conversion is determined by the Device Wake-up bits in the USB Timing register. All other behaviors of Audio

Type 1 and other accessories will not be affected by the RAW DATA bit. LKR and the button bits will not set when RAW DATA = 0. The period of ADC conversion is determined by the Device Wake-up bits in the Timing Set 1 register. All other behaviors of Audio Type 1 and other accessories will not be affected by the RAW DATA bit.

7.8.4.7 Analog and Digital Switches

The signal switches in the MC34708 are shown in Figure 26. These switches are controlled by the identification result when the Manual S/W = 1, and by the Manual SW/Result register, when the Manual S/W = 0 is in Active mode. The Switch_Open bit overrides the switch configuration. When the Switch_Open bit is 0, all switches are turned off. The switches for the SPK_L and SPK_R are capable of passing signals of ±1.5 V, referencing to the GND pin voltage. The SPK_L and SPK_R pins are pulled down to GND via a 100 kΩ resistor respectively, as shown in Figure 26. When the switches are configured automatically by the identification result, the configuration of the switches vs. the device type is shown in Table 93.

When detachment of an accessory is detected, the MC34708 will return to Standby mode. In Standby mode, regardless of the Manual S/W = 1 or Manual S/W = 0 state, all signal switches and are off in the Standby mode. The OUT-to-ground FET is turned on whenever the FET_ON bit is '0'.

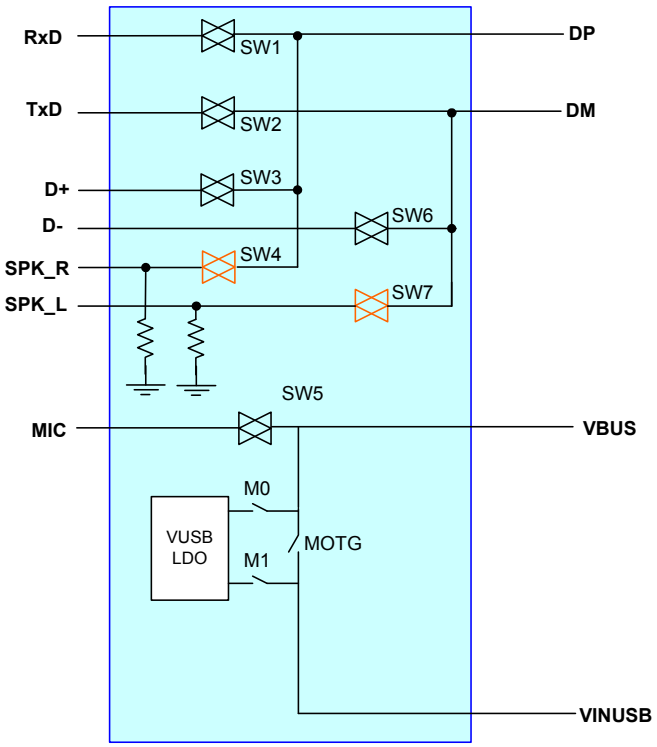


Figure 26. Analog and Digital Switches

Table 93. Switch Configuration When Controlled by the Device Type Register

Device Type	Audio	USB	UART	USB CHG	Dedicated CHG
On SW#	4, 5, 7	3, 6,	1, 2	3, 6	-
Off SW	MOTG, M0	-	(70)	-	-
Device Type	5WT1 CHG	5WT2 CHG	JIG_USB_ON JIG_USB_OFF	JIG_UART_ON JIG_UART	TTY
On SW#	-	-	3, 6	3, 6	4, 5, 7
Off SW	-	-	-	(70)	MOTG, M0

Notes

70. Switches M0, M1, and MOTG are controlled by software by the OTGEN and VUSBSEL bits.

7.8.4.8 Audio Type 1 Operation Mode

Audio Type 1 accessories have the same interface shown in Figure 27, either stereo or mono, with or without a remote control, or with or without a microphone. When a device, such as a microphone is not connected to the accessory, the corresponding pin in the mini-USB connector will be left floating. With the normal operation setting of the control bits, the accessory is identified as an Audio Type 1 device, the analog switches SW4 and SW7 for SPK_R to DP, SPK_L to DM, and SW5 for VBUS to MIC are turned on, and the MOTG, and M0 switches are turned off, to isolate the VBUS pin.

The MC34708 supports the remote control key for an Audio Type 1 device. If the RAW DATA = 0, the ADC is turned on periodically to monitor the ID line change caused by the key press. The period is programmed by the Device Wake-up bits. If the ADC Result changes, the ADC_Change bit in the USB Interrupt Sense register is set to inform the baseband. If the RAW DATA = 1, a comparator is enabled to monitor the key press. The timing of the key press when RAW DATA = 1 is shown in Figure 28. If a key is pressed for a time less than 20 ms, the MC34708 ignores it. If the key is still pressed after 20 ms, the MC34708 starts a timer to count the time during which the key is kept pressed. There are three conditions according to the press time: Error key press, short key press, and long key press.

1. Error key press: if the key press time is less than TKP, the Error bit in the USB Button register and the short key press bit KP in USB Interrupt Sense register are set to indicate an error has occurred. The Error bit is reset to '0' when the USB Button register is read or the next key press occurs. The KP bit is cleared when the Interrupt 1 register is read.
2. Short key press: if the key press time is between TKP and TLKP, the KP bit and the corresponding button bit in USB Button are set to inform the baseband. If the ADC result is not one of the ADC values of the 13 buttons, the Unknown bit in the Button register is set. The INT pin is driven high when the key is released and returns to low when the interrupt register is read. The KP bit is cleared when the USB Interrupt Sense register is read.
3. Long key press: if the key press time is longer than TLKP, the long key press bit LKP in the USB Interrupt Sense register, and the corresponding button bit, are set to inform the baseband. If the ADC Result is not one of the ADC values of the 13 buttons, the Unknown bit in the USB Button register is set. When the key is released, the long key release bit LKR in the Interrupt Status 0 register is set to interrupt the baseband again.

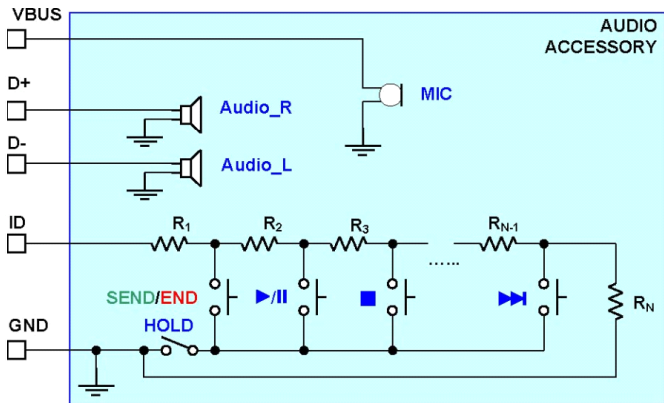


Figure 27. Audio Accessory with Remote Control and Microphone

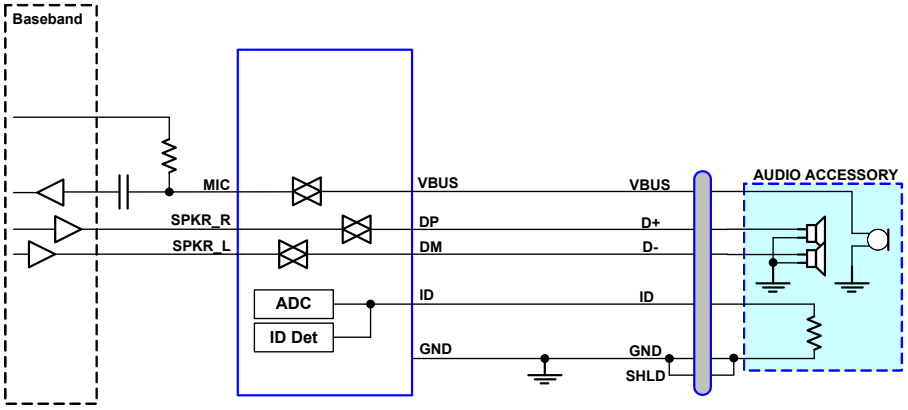


Figure 28. Operation of the Headset with Remote Control and Microphone

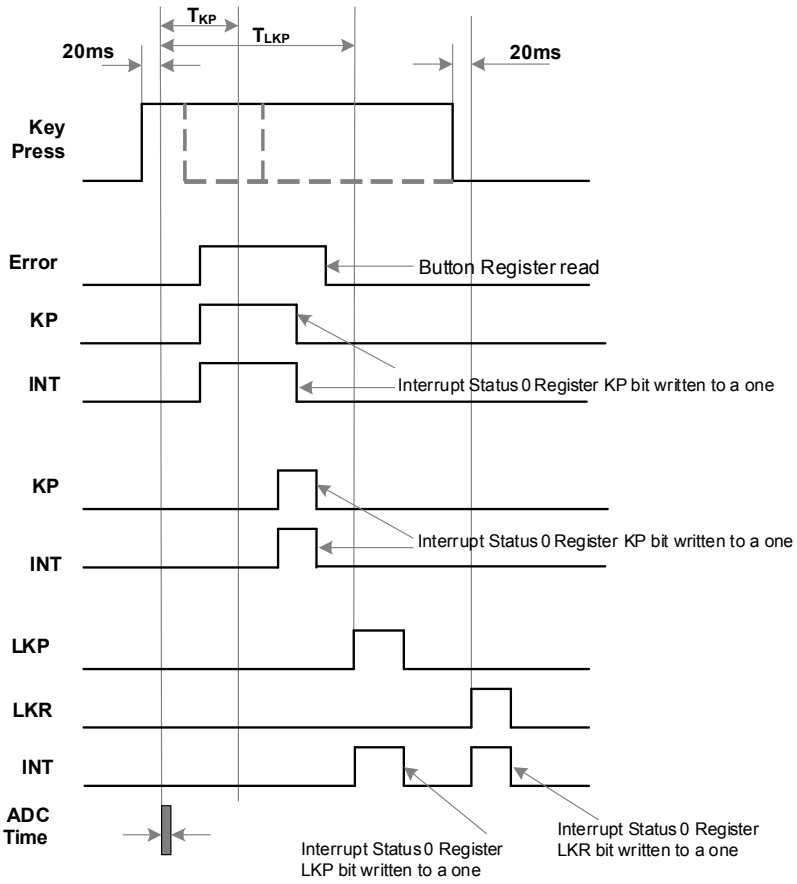


Figure 29. Remote Control Key Press Timing

The ID detection circuit continues to be ON for detaching detection in the Active mode, and samples the ID line every interval programmed by the device wake-up bits in the USB Timing register. When the ID_FLOAT rising edge is detected, the Detach bit in the USB Interrupt Sense register is set to inform the host the accessory is detached. The MC34708 then enters Standby mode.

7.8.4.9 JiG Cable USB and UART

The JIG cable is used for test and development and has an ID resistance to differentiate it from a regular USB cable. The Jig cable has 2 ID resistance values to resemble a USB JIG type1/2, and 2 ID resistance values to resemble a UART JIG type1/2 cable.

7.8.4.9.1 USB JIG Cable 1 or 2

Under normal operation, setting the control bits when the identified accessory is a USB JIG 1 or 2 cable, both the DPLUS to DP, the DMINUS to DM switches are switched on.

When SW_HOLD = 0, the switching action of DPLUS to DP, and the DMINUS to DM switches are controlled by the WAIT bit. If WAIT = 1, the signal switches will be turned ON after a WAIT. If WAIT = 0, the signal switches won't be turned on until the WAIT bit is set to '1' by the SPI/I^2C. When SW_HOLD = 1, regardless of what the WAIT is set to, '0' or '1', the signal switches are turned on, once the USB JIG cable is identified.

The ID detector and the VBUS detector both monitor the detachment of the USB JIG cable. The ID detection circuit continues to be ON for detachment detection in the Active mode. When the ID_FLOAT is set, the Detach bit in the Interrupt Status 0 register is set to inform the host. When the USBDETS is set to '0', which means either the VBUS power is removed or the cable is detached, the Detach bit is also set to inform the host. The mini USB interface moves to the Standby mode. If the Detach bit is set, due to the removing only the VBUS or the ID resistance, and the cable is not detached completely, the identification flow will be triggered again. The ID_FLOAT bit or USBDETS bit still indicate an accessory is connected when the mini USB interface moves to the Standby mode. All the signal switches are turned off

7.8.4.9.2 UART JIG Cable 1 or 2

Under normal operation, setting the control bits when the identified accessory is a UART JIG cable 1 or 2, both the RxD to DP and the TxD to DM switches are switched on.

When SW_HOLD = 0, the switching action of RxD to DP, and the TxD to DM switches, are controlled by the WAIT bit. If WAIT = 1, the signal switches will be turned on after a WAIT time. If WAIT = 0, the signal switches won't be turned on until the WAIT bit is set to '1' by the SPI/I^2C. When SW_HOLD = 1, regardless of what the WAIT is set to, '0' or '1', the signal switches are turned on, once the UART JIG cable is identified.

The ID detection comparator continues to be ON for detachment detection in the Active mode. When the ID_FLOAT is set, the Detach bit in the Interrupt Status 0 register is set to inform the host the accessory is detached. The mini USB interface then enters the Standby mode.

7.8.4.10 TTY Operation Mode

A TTY converter is a type of audio accessory. It has its own ID resistance. When a TTY converter is attached, this sets the TTY bit in the USB Device Type register and the Attach interrupt bit in the Interrupt Status 0 register. During normal operation, when setting the control bits, the automatic switch configuration of the TTY converter, is similar to that of an Audio Type 1 accessory. The SPK_R to DP switch, and MIC to VBUS switch are turned on, but the SPK_L to DM switch can only be turned on when TTY_SKPL bit in USB Control register is manually set to 1. In addition, the MOTG, and M0 switches are turned off to isolate the VBUS pin.The TTY accessory doesn’t support the remote control key. The Power Save mode operation and the detachment detection are the same as those of the Audio Type 1 device.

7.8.4.11 UART Operation Mode

During normal operation, when setting the control bits, when the identified accessory is a UART cable, both the RxD and the TxD switches are switched on (see Figure 30).

The ID detection comparator continues to be ON for detachment detection in the Active mode. When the ID_FLOAT is set, the Detach bit in the USB interrupt Sense register, is set to inform the host the accessory is detached. The MC34708 USB detection then enters Standby mode.

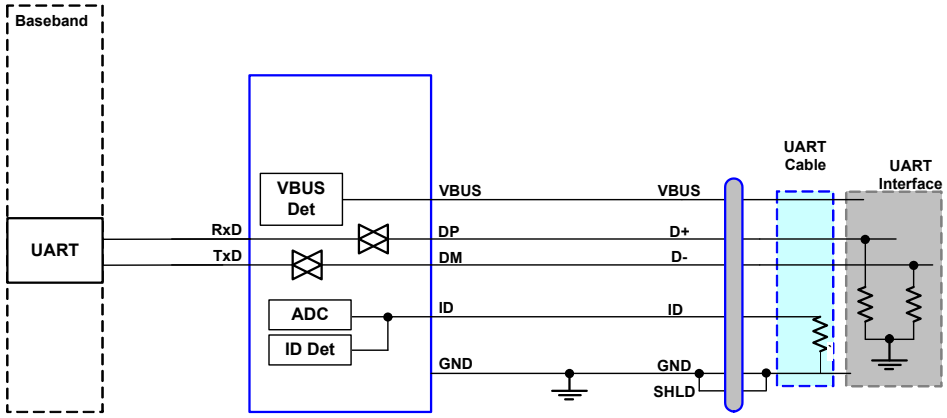


Figure 30. UART Operation

7.8.4.12 USB Host (PC or HUB) Operation Mode

When the attached accessory is a USB host or hub, the ID pin floats. During normal operation, when setting the control bits, both the D PLUS to DP and the D MINUS to DM switches are switched on (see Figure 31). The mini USB interface sets the bit USB in the USB Device type register.

When SW_HOLD = 0, the switching action of D+ to DP and the D- to DM switches, are controlled by the WAIT bit. If WAIT = 1, the signal switches will be turned on after a WAIT time. If WAIT = 0, the signal switches won't be turned on until the WAIT bit is set to '1' by the SPI. When SW_HOLD = 1, regardless of what the WAIT is set to, '0' or '1', the signal switches are turned on once the USB host is identified.

After the DPLUS to DP and the DMINUS to DM switches are turned on, the baseband can pull the DPLUS signal high to start the USB attaching sequence.

The detachment is detected by the falling edge of the USBDETS signal. When the USBDETS falls, the Detach bit is set to inform the baseband. The MC34708 USB detection then enters the Standby mode.

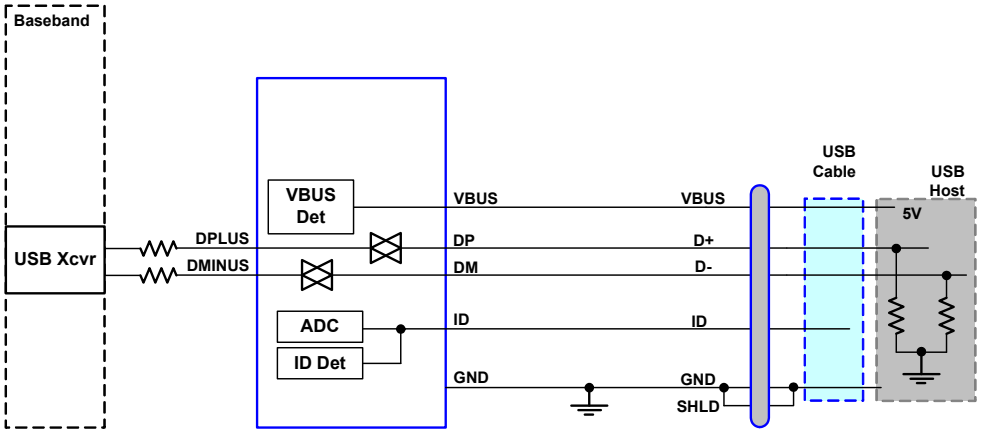


Figure 31. USB Operation

7.8.4.13 USB charger or Dedicated Charger Operation Mode

When the attached accessory is a USB Charger or Dedicated Charger, the MC34708 enables the bit USB Charge or the Dedicated CHG in the USB Device type register. During normal operation when setting of the control bits, the D PLUS and D MINUS switches are turned on for the USB Charger, but not for the Dedicated Charger.

The VBUS detector is used to monitor the detachment of the charger. The falling edge of USBDETS is an indication of charger detachment. Unplugging the mini-USB connector and unplugging the AC side, both lead to the same detachment conclusion. The Detach bit is set to inform the host. The MC34708 USB detection then enters the Standby mode.

7.8.4.14 5-Wire Charger or A/V Charger Mode

When the attached accessory is a 5-Wire Charger or A/V Charger, the MC34708 enables the appropriate device type 5.0 W CHG or A/V in the USB device type register.

The VBUS detector is used to monitor the detachment of the charger. The falling edge of USBDETS is an indication of the charger detachment. Both unplugging the mini-USB connector and unplugging the ac side lead to the same detachment conclusion. The Detach bit is set to inform the host. Then the MC34708 USB detection enters the Standby mode.

7.8.4.15 Device Detect Mode

When the Manual SW_B bit is set to 1, the MC34708 automatically detects what device is attached.

7.8.4.16 Unknown Accessory Operation Mode

When an unknown accessory is attached, the ID_FLOAT bit is cleared or the USBDETS bit is set to '1'. Only the Unknown_Atta bit is set to interrupt the baseband. The Attach bit is not set to distinguish the unknown accessory from the known accessory. No other actions are taken.The falling edge of the USBDETS or the rising edge of the ID_FLOAT signals can trigger the detachment detection. The Detach bit is set to inform the detachment of the unknown accessory. The USB detection then enters the Standby mode.

7.8.4.17 Software Reset

The USB detection supports a software reset, which is realized by writing the Reset bit in the USB Control register to 1. The consequence of the software reset is the same as the hardware reset. All register bits reset by the Mini-USB will be reset.

Table 94. ID Detection Thresholds

UID Pin External Connection	UID Pin Voltage [71]	IDFLOATS	IDGNDS	IDFACTORYS	Accessory
Resistor to Ground	0.18 * VCORE < UID < 0.77 * VCORE	0	1	0	Non-USB accessory is attached (per CEA-936-A spec)
Grounded	0 < UID < 0.12 * VCORE	0	0	0	A type plug (USB default slave) is attached (per CEA-936-A spec)
Floating	0.89 * VCORE < UID < VCORE	1	1	0	B type plug (USB Host, OTG default master or no device) is attached.
Voltage Applied	3.6 V < UID (1)	1	1	1	Factory mode

Notes
71. UID maximum voltage is 5.25 V

7.8.4.18 ID Resistance Value Assignment

The ID resistors used are standard 1% resistors. Table 95 lists the complete 32 ID resistor assignment. Those with the Assigned Functions filled are ones already used with special functions. The ones reserved can be assigned to other functions.

Table 95. ID Resistance Assignment

Item#	ADC Result	ID Resistance KΩ	Assignment
0	00000	<1.9	Reserved
1	00001	2.0	S0
2	00010	2.604	S1
3	00011	3.208	S2
4	00100	4.014	S3

Table 95. ID Resistance Assignment

Item#	ADC Result	ID Resistance KΩ	Assignment
5	00101	4.820	S4
6	00110	6.03	S5
7	00111	8.03	S6
8	01000	10.03	S7
9	01001	12.03	S8
10	01010	14.46	S9
11	01011	17.26	S10
12	01100	20.5	S11
13	01101	24.07	S12
14	01110	28.7	UART JIG Cable 2
15	01111	34.0	UART JIG Cable 1
16	10000	40.2	USB JIG Cable 2
17	10001	49.9	USB JIG Cable 1
18	10010	64.9	Factory Mode
19	10011	80.6	Audio Type 2
20	10100	102	PPD
21	10101	121	Reserved
22	10110	150	UART
23	10111	200	5W Type 1
24	11000	255	Reserved
25	11001	301	Reserved
26	11010	365	A/V
27	11011	442	5W Type 2
28	11100	523	Reserved
29	11101	619	TTY
30	11110	1000	Audio Type 1
31	11111	-	ID float

The remote control architecture is illustrated in Figure 32. The recommended resistors for the remote control resistor network are given in Table 96.

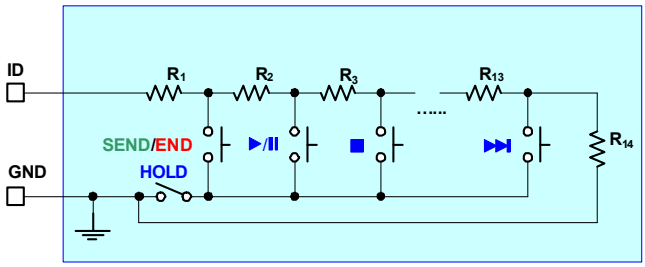


Figure 32. Remote Control Architecture

Table 96. ID Remote Control Values

Resistor	Standard Value KΩ	ID Resistance
R1	2.0	2.0
R2	0.604	2.604
R3	0.604	3.208
R4	0.806	4.014
R5	0.806	4.82
R6	1.21	6.03
R7	2.0	8.03
R8	2.0	10.03
R9	2.0	12.03
R10	2.43	14.46
R11	2.8	17.26
R12	3.24	20.5
R13	3.57	24.07
R14	590/976	614/1000

7.8.4.19 USB Interface Electrical Specifications

Table 97. USB Interface Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power Input						
I_{DM}	Detection Module Quiescent Current				μA	
	• In Standby mode	-	2	3		
	• When accessory is attached & INT_MASK = '1'	-	125	160		
	• In Active mode (V_{DD} < V_{BUS})	-	550	650		
	• In Active mode (V_{DD} < V_{BUS})	-	850	1000		
I_{VBUS}	VBUS Supply Quiescent Current				mA	
	• In VBUS OTG	-	-	1.5		
	• In Active mode - Audio or TTY	-	-	0.5		
Accessory Detect Switch						
	SPK_L and SPK_R Switches				Ω	
R_{SPK_ON}	• On resistance (20 Hz to 470 kHz)	-	30	-		
R_{SPK_ONMCT}	• Matching between channels	-	3.0	-		
R_{SPK_ONFLT}	• On resistance flatness (from -1.2 to 1.2 V)	-	0.3	-		
	D+ and D- Switches				Ω	
R_{USB_ON}	• On resistance (0.0 Hz to 240 MHz)	-	5.0	8.0		
R_{USB_ONMCT}	• Matching between channels	-	0.1	1.0		
R_{USB_ONFLT}	• On resistance flatness (from 0.0 to 3.3 V)	-	0.02	0.4		

Table 97. USB Interface Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
	RxD and TxD Switches				Ω	
R_{UART_ON}	• On resistance	-	-	60		
R_{UART_ONFLT}	• On resistance flatness (from 0.0 to 3.3 V)	-	-	6.0		
	MIC Switches				Ω	
R_{MIC_ON}	• On resistance (at 1.5 V MIC bias voltage)	-	75	150		
R_{PD_AUDIO}	Pull-Down Resistors between SPK_L or SPK_R Pins to GND	-	100	-	kΩ	
	Signal Voltage Range				V	
	• MIC	-	-	1.5		
	• SPK_L, SPK_R	-1.5	-	1.5		
	• D+, D-, RxD, TxD	-0.3	-	3.6		
V_{A_PSRR}	PSRR - From BP (100 mVrms) to DP/DM Pins				dB	
	• 20 Hz to 20 kHz with 32/16 Ω load.	-	-	-60		
T_{HD}	Total Harmonic Distortions				%	
	• 20 Hz to 20 kHz with 32/16 Ω load.	-	-	0.05		
V_{A_CT}	Crosstalk between Two Channels				dB	
	• 20 Hz to 20 kHz with 32/16 Ω load.	-	-	-50		
V_{A_ISO}	Off Channel Isolation				dB	
	• Less than 1.0 MHz	-	-	-100		
Power Supply Type Identification						
V_{DAT_SRC}	Data Source Voltage				V	
	• Loaded by 0~200 µA	0.5	0.6	0.7		
I_{DAT_SRC}	Data Source Current	0.0	-	200	µA	
V_{DAT_REF}	Data Detect Voltage	0.3	0.35	0.4	V	
V_{CR_REF}	Car Kit Detect Voltage	0.8	0.9	1.0	V	
I_{DAT_SINK}	Data Sink Current				µA	
	• DM pin is biased between 0.15 to 3.0 V	65	100	135		
$C_{DP/DM}$	DP, DM Pin Capacitance	-	8.0	-	pF	
$R_{DP/DM}$	DP, DM Pin Impedance				MΩ	
	• All switches are off (Switch_Open = 0)	-	50	-		
ID Detection						
V_{FLOAT}	ID FLOAT Threshold				V	
	• Detection threshold	-	2.3	-		
t_{ID_FLOAT}	ID FLOAT Detection Deglitch Time	-	20	-	ms	
IID	Pull-up Current Source				µA	
	• When ADC Result is 1xxxx	1.9	2.0	2.1		
	• When ADC Result is 0xxxx	30.4	32	33.6		
	Video Cable Detection					
I_{VCBL}	• Detection current	1.0	1.2	1.4	mA	
V_{VCBL_L}	• Detection voltage low threshold	-	50	-	mV	
V_{VCBL_H}	• Detection voltage high threshold	-	118	-	mV	

Table 97. USB Interface Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
ID Detection (Continued)						
t_{VCBL}	Video Cable Detection Time (Video Cable Detection Current Source On Time)	-	20	-	ms	
t_{RMTCON_DG}	Key Press Comparator Debounce Time	-	20	-	ms	

7.9 Serial Interfaces

The IC contains a number of programmable registers for control and communication. The majority of registers are accessed through a SPI interface in a typical application. The same register set may alternatively be accessed with an I^2C interface muxed on SPI pins. Table 98 describes the muxed pin options for the SPI and I^2C interfaces; further details for each interface mode follow.

Table 98. SPI / I^2C Bus Configuration

Pin Name	SPI Mode Functionality	I^2C Mode Functionality
CS	Configuration (72), Chip Select	Configuration (73)
CLK	SPI Clock	SCL: I^2C bus clock
MISO	Master In, Slave Out (data output)	SDA: Bi-directional serial data line
MOSI	Master Out, Slave In (data input)	A0 Address Selection (74)

Notes

72. CS held low at Cold Start, configures the interface for SPI mode; once activated, CS functions as the SPI Chip Select.
73. CS tied to VCOREDIG at Cold Start, configures the interface for I^2C mode; the pin is not used in I^2C mode, other than for configuration.
74. In I^2C mode, the MOSI pin is hardwired to ground, or VCOREDIG is used to select between two possible addresses.

7.9.1 SPI Interface

The IC contains a SPI interface port which allows access by a processor to the register set. Via these registers, the resources of the IC can be controlled. The registers also provide status information about how the IC is operating, as well as information on external signals.

Because the SPI interface pins can be reconfigured for reuse as an I^2C interface, a configuration protocol mandates the CS pin is held low during a turn on event for the IC (a weak pull-down is integrated on the CS pin). The state of CS is latched in during the initialization phase of a Cold Start sequence, ensuring the I^2C bus is configured before the interface is activated. With the CS pin held low during startup (as would be the case if connected to the CS driver of an unpowered processor due to the integrated pull down), the bus configuration will be latched for SPI mode.

The SPI port utilizes 32-bit serial data words comprised of 1 write/read_b bit, 6 address bits, 1 null bit, and 24 data bits. The addressable register map spans 64 registers of 24 data bits each. The map is not fully populated, but it follows the legacy conventions for bit positions corresponding to common functionality with previous generation FSL products.

7.9.1.1 SPI Interface Description

For a SPI read, the first bit sent to the IC must be a zero indicating a SPI read cycle. Next, the six bit address is sent MSB first. This is followed by one dead bit to allow for more address decode time. The MC34708 will clock the above bits in on the rising edge of the SPI clock. The 24 data bits are then driven out on the MISO pin on the falling edge of the SPI clock, so the master can clock them in on the rising edge of the SPI clock.

For each MOSI SPI transfer, first a one is written to the write/read_b bit if this SPI transfer is to be a write. A zero is written to the write/read_b bit if this is to be a read command. If a zero is written, then any data sent after the address bits are ignored and the internal contents of the field addressed do not change when the 32nd CLK is sent.

For a SPI write, the first bit sent to the MC34708 must be a one, indicating a SPI write cycle. Next the six bit address is sent MSB first. This is followed by one dead bit to allow for more address decode time. The data is then sent MSB first. The SPI data is written to the SPI register whose address was sent at the start of the SPI cycle on the falling edge of the 32nd SPI clock. Additionally, whenever a SPI write cycle is taking place the SPI read data is shifted out for the same address as for the write cycle. Next the 6-bit address is written, MSB first. Finally, data bits are written, MSB first. Once all the data bits are written then the data is transferred into the actual registers on the falling edge of the 32nd CLK.

The CS polarity is active high. The CS line must remain high during the entire SPI transfer. For a write sequence it is possible for the written data to be corrupted, if after the falling edge of the 32nd clock the CS goes low before it's required time. CS can go low before this point and the SPI transaction will be ignored, but after that point the write process is started and cannot be stopped, because the write strobe pulse is already being generated, and CS going low may cause a runt pulse that may or may not be wide enough to clock all 24 data bits properly. To start a new SPI transfer, the CS line must be toggled low and then pulled high again. The MISO line will be tri-stated while CS is low.

The register map includes bits that are read/write, read only, read/write “1” to clear (i.e., Interrupts), and clear on read, reserved, and unused. Refer to the SPI/I2C Register Map and the individual subcircuit descriptions to determine the read/write capability of each bit. All unused SPI bits in each register must be written to as zeroes. A SPI read back of the address field and unused bits are returned as zeroes. To read a field of data, the MISO pin will output the data field pointed to by the 6 address bits loaded at the beginning of the SPI sequence.

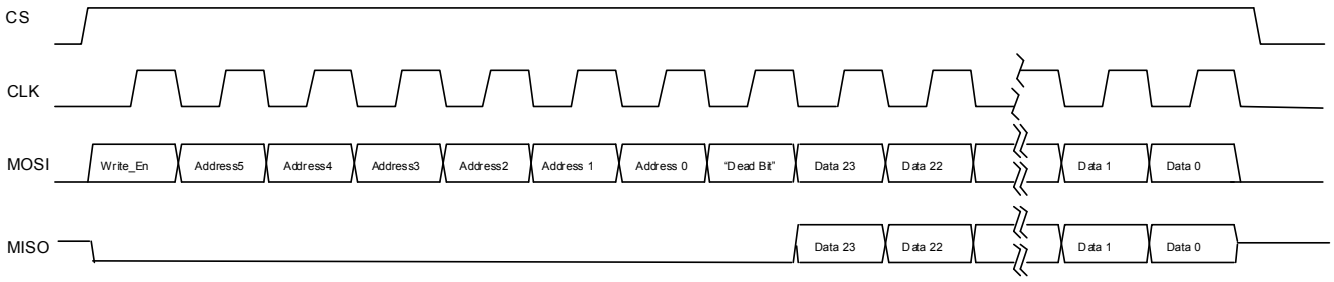


Figure 33. SPI Transfer Protocol Single Read/Write Access

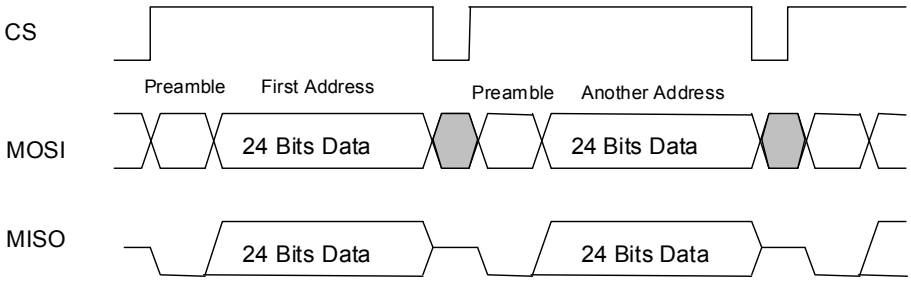


Figure 34. SPI Transfer Protocol Multiple Read/Write Access

7.9.1.2 SPI Timing Requirements

The following diagram and table summarize the SPI timing requirements. The SPI input and output levels are set via the SPIVCC pin, by connecting it to the desired supply. This would typically be tied to SW5 and programmed for 1.80 V. The strength of the MISO driver is programmable through the SPIDRV [1:0] bits. See Thermal Protection Thresholds for detailed SPI electrical characteristics.

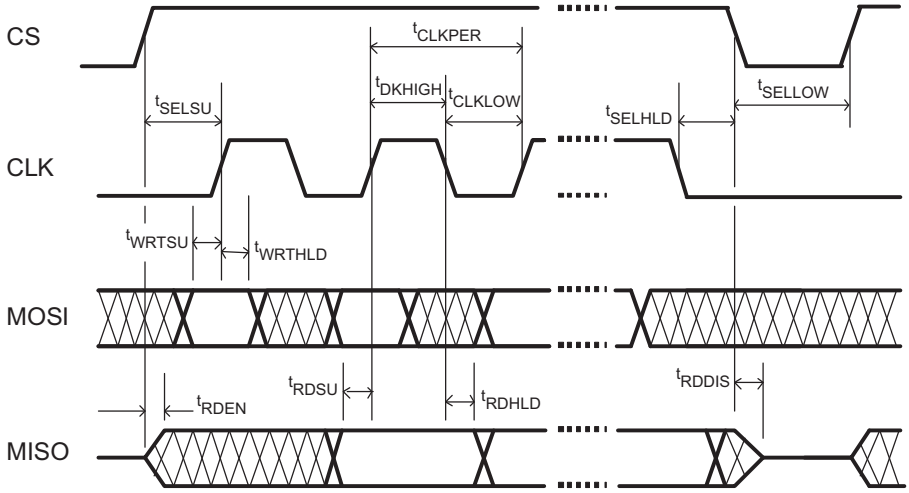


Figure 35. SPI Interface Timing Diagram

Table 99. SPI Interface Timing Specifications[75]

Parameter	Description	T min (ns)
t_{SELSU}	Time CS has to be high before the first rising edge of CLK	15
t_{SELHLD}	Time CS has to remain high after the last falling edge of CLK	15
t_{SELLOW}	Time CS has to remain low between two transfers	15
t_{CLKPER}	Clock period of CLK	38
$t_{CLKHIGH}$	Part of the clock period where CLK has to remain high	15
t_{CLKLOW}	Part of the clock period where CLK has to remain low	15
t_{WRTSU}	Time MOSI has to be stable before the next rising edge of CLK	4.0
t_{WRTHLD}	Time MOSI has to remain stable after the rising edge of CLK	4.0
t_{RDSU}	Time MISO will be stable before the next rising edge of CLK	4.0
t_{RDHLD}	Time MISO will remain stable after the falling edge of CLK	4.0
t_{RDEN}	Time MISO needs to become active after the rising edge of CS	4.0
t_{RDDIS}	Time MISO needs to become inactive after the falling edge of CS	4.0

Notes
75. This table reflects a maximum SPI clock frequency of 26 MHz.

7.9.2 I²C Interface

7.9.2.1 I²C Configuration

When configured for I²C mode, the interface may be used to access the complete register map previously described for SPI access. Since SPI configuration is more typical, references within this document will generally refer to the common register set as a “SPI map” and bits as “SPI bits”; however, it should be understood that access reverts to I²C mode when configured as such.

The SPI pins CLK and MISO are reused for the SCL and SDA lines respectively. Selection of I²C mode for the interface is configured by hard-wiring the CS pin to VCOREDIG on the application board. The state of CS is latched in during the initialization phase of a Cold Start sequence, so the I²CS bit is defined for bus configuration before the interface is activated. The pull-down on CS will be deactivated if the high state is detected (indicating I²C mode).

In I²C mode, the MISO pin is connected to the bus as an open drain driver, and the logic level is set by an external pull-up. The part can function only as an I²C slave device, not as a host.

7.9.2.2 I²C Device ID

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. To allow flexibility in addressing for bus conflict avoidance, pin programmable selection is provided to allow configuration for the address LSB(s). This product supports 7-bit addressing only; support is not provided for 10-bit or general Call addressing.

Because the MOSI pin is not utilized for I²C communication, it is reassigned for pin programmable address selection by hardwiring to VCOREDIG or GND at the board level when configured for I²C mode. MOSI will act as Bit 0 of the address. The I²C address assigned to FSL PM ICs (shared amongst our portfolio) is given as follows:

00010-A1-A0, the A1 and A0 bits are allowed to be configured for either 1 or 0. The A1 address bit is internally hardwired as a “0”, leaving the LSB A0 for board level configuration. The designated address then is defined as: 000100-A0.

7.9.2.3 I²C Operation

The I²C mode of the interface is implemented generally following the Fast Mode definition which supports up to 400 kbits/s operation. (Exceptions to the standard are noted to be 7-bit only addressing, and no support for general Call addressing) Timing diagrams, electrical specifications, and further details on this bus standard, is available on the internet, by typing “I²C specification” in the web search string field.

Standard I²C protocol utilizes bytes of 8 bits, with an acknowledge bit (ACK) required between each byte. However, the number of bytes per transfer is unrestricted. The register map is organized in 24 bit registers which corresponds to the 24 bit words supported by the SPI protocol of this product. To ensure that I²C operation mimics SPI transactions in behavior of a complete 24 bit word being written in one transaction, software is expected to perform write transactions to the device in 3-byte sequences, beginning with the MSB. Internally, data latching will be gated by the acknowledge at the completion of writing the third consecutive byte.

Failure to complete a 3-byte write sequence will abort the I²C transaction and the register will retain its previous value. This could be due to a premature STOP command from the master, for example.

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and 3-bytes will be sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device will respond to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NAK is received, the host should terminate the current transaction and retry the transaction.

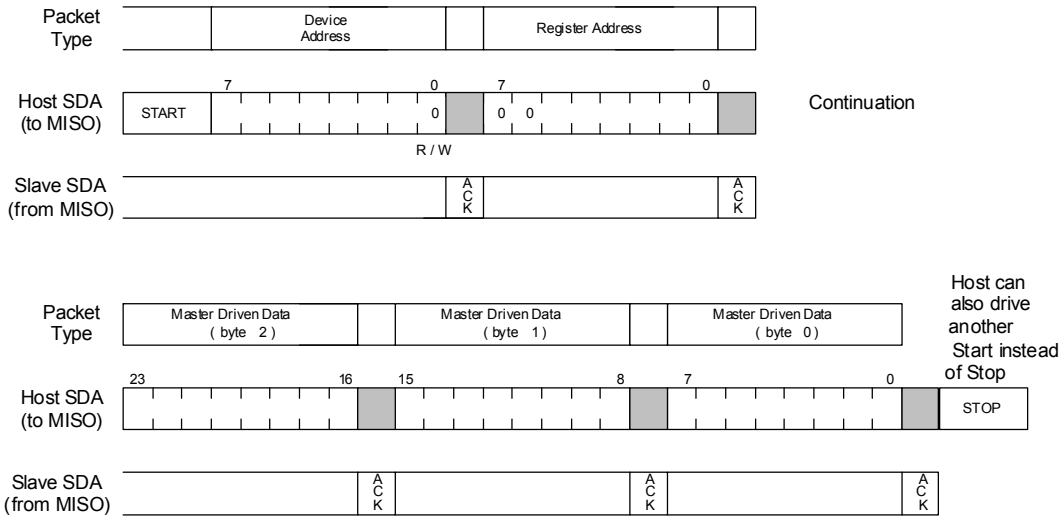


Figure 36. I²C 3-byte Write Example

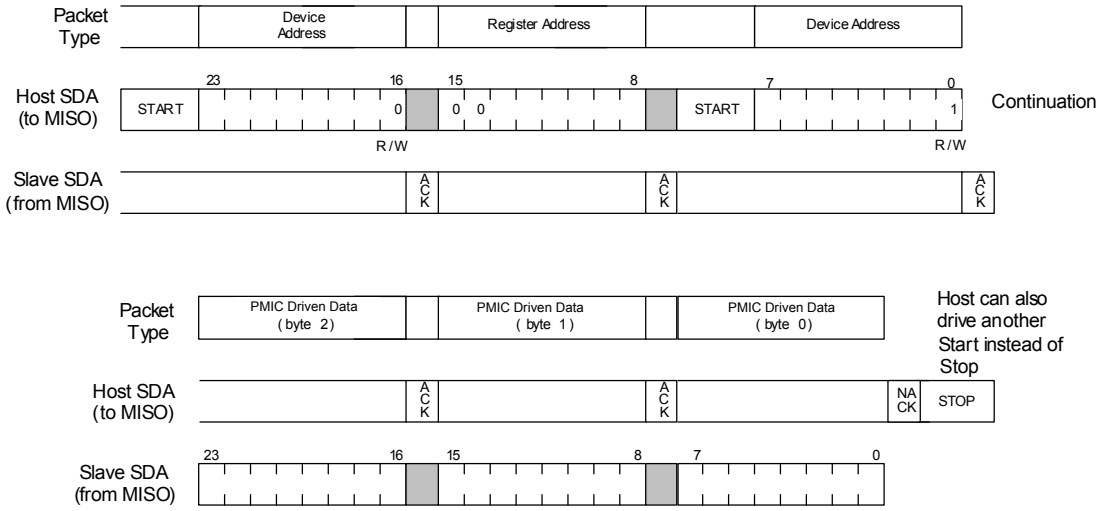


Figure 37. I²C 3-byte Read Example

7.9.3 SPI/I²C Specification

Table 100. SPI/I²C Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, V_{BUS} = 5.0 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SPI Interface Logic IO						
V_{INCSLO}	Input Low CS	0.0	-	0.4	V	
V_{INCSHI}	Input High CS	1.1	-	SPIVCC+0.3	V	
$V_{INMOSILO}$/ $V_{INCLKLO}$	Input Low, MOSI, CLK	0.0	-	0.3*SPIVCC	V	
$V_{INMOSIHI}$/ $V_{INCLKHI}$	Input High, MOSI, CLK	0.7*SPIVCC	-	SPIVCC+0.3	V	
V_{MISOLO}/ V_{INTLO}	Output Low MISO, INT • Output sink 100 μA	0.0	-	0.2	V	
V_{MISOHI}/ V_{INTHI}	Output High MISO, INT • Output source 100 μA	SPIVCC-0.2	-	SPIVCC	V	
V_{CC-SPI}	SPIVCC Operating Range	1.75	-	3.6	V	
t_{MISOET}	MISO Rise and Fall Time, CL = 50 pF, SPIVCC = 1.8 V				ns	
	• SPIDRV [1:0] = 00	-	6.0	-		
	• SPIDRV [1:0] = 01 (default)	-	2.5	-		
	• SPIDRV [1:0] = 10	-	3.0	-		
	• SPIDRV [1:0] = 11	-	2.0	-		

7.10 Configuration Registers

7.10.1 Register Set structure

The general structure of the register set is given in the following table. Expanded bit descriptions are included in the following functional sections for application guidance. For brevity's sake, references are occasionally made herein to the register set as the "SPI map" or "SPI bits", but note that bit access is also possible through the I²C interface option so such references are implied as generically applicable to the register set accessible by either interface.

Table 101. Register Set

	Register		Register		Register		Register
0	Interrupt Status 0	16	Memory A	32	Regulator Mode 0	48	ADC5
1	Interrupt Mask 0	17	Memory B	33	GPIOLV0 Control	49	ADC6
2	Interrupt Sense 0	18	Memory C	34	GPIOLV1 Control	50	ADC7
3	Interrupt Status 1	19	Memory C	35	GPIOLV2 Control	51	Input Monitoring
4	Interrupt Mask 1	20	RTC Time	36	GPIOLV3 Control	52	Supply Debounce
5	Interrupt Sense 1	21	RTC Alarm	37	USB Timing	53	VBUS monitoring
6	Power Up Mode Sense	22	RTC Day	38	USB Button	54	LED Control
7	Identification	23	RTC Day Alarm	39	USB Control	55	PWM Control
8	Regulator Fault Sense	24	Regulator 1 A/B Voltage	40	USB Device Type	56	Unused

Table 101. Register Set

	Register		Register		Register		Register
9	Reserved	25	Regulator 2 & 3 Voltage	41	Unused	57	Unused
10	Reserved	26	Regulator 4 A/B Voltage	42	Unused	58	Unused
11	Reserved	27	Regulator 5 Voltage	43	ADC 0	59	Unused
12	Unused	28	Regulator 1 & 2 Mode	44	ADC 1	60	Unused
13	Power Control 0	29	Regulator 3, 4 and 5 Mode	45	ADC 2	61	Unused
14	Power Control 1	30	Regulator Setting 0	46	ADC 3	62	Unused
15	Power Control 2	31	SWBST Control	47	ADC4	63	Unused

7.10.2 Specific Registers

7.10.2.1 IC and Version Identification

The IC and other version details can be read via the identification bits. These are hardwired on the chip and described in Table 102.

Table 102. IC Revision Bit Assignment

Identifier	Value	Purpose
FULL_LAYER_REV[2:0]	XXX	Represents the full layer revision • Pass 2.4 = 010
METAL_LAYER_REV[2:0]	XXX	Represents the metal layer revision • Pass 2.4 = 100
FIN[2:0]	000	FIN version • Pass 2.4 = 000
FAB[2:0]	000	FAB Version • Pass 2.4 = 000

7.10.2.2 Embedded Memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[23:0], MEMB[23:0], MEMC[23:0], and MEMD[23:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut). The contents of the embedded memory are reset by RTCPORB. A known pattern can be maintained in these registers to validate confidence in the RTC contents when power is restored after a power cut event. Alternatively, the banks can be used for any system need for bit retention with coin cell backup.

7.10.3 SPI/I²C Register Map

The complete SPI bitmap is given in Table 103.

Table 103. SPI/I²C Register Map Legend

Register Types	
R/W	Read / Write
R/WM	Read / Write Modify
W1C	Write One to Clear
RO	Read Only
NU	Not Used

Register Values
0 = low
1 = High
X = Variable

Reset
Bits Loaded at Cold Start based on PUMS Value
Bits Reset by POR or Global Reset
RESETB / Bits Reset by POR or Global
Bits Reset by RTCPORB or Global Reset
Bits Reset by POR or OFFB
Bits Reset by RTCPORB Only
MUSBRST

Table 104. SPI/I²C Register Map

Address	Register Name	Type	Default	MC34708 SPI Register Map							
0	Interrupt Status 0 Table 105	W1C	h00_00_00	23	22	21	20	19	18	17	16
				STUCK_KEY_RCV	STUCK_KEY	ADC_CHANGE	UNKNOWN_ATTA	LKR	LKP	KP	DETACH
				15	14	13	12	11	10	9	8
				ATTACH	-	LOWBATT	-	-	-	-	-
				7	6	5	4	3	2	1	0
				-	-	USBOVP	-	USBDET	TSPENDET	TSDONEI	ADCDONEI
1	Interrupt Mask 0 Table 106	R/W	hFF_FF_FF	23	22	21	20	19	18	17	16
				STUCK_KEY_RCV_M	STUCK_KEY_M	ADC_CHANGE_M	UNKNOWN_ATTA_M	LKR_M	LKP_M	KP_M	DETACH_M
				15	14	13	12	11	10	9	8
				ATTACH_M	-	LOWBATTM	-	-	-	-	-
				7	6	5	4	3	2	1	0
				-	-	USBOVPM	-	USBDETM	TSPENDETM	TSDONEM	ADCDONEM
2	Interrupt Sense 0 Table 107	RO	h00_00_00	23	22	21	20	19	18	17	16
				-	-	MUSB_ADC_STATUS	ID_GNDS	ID_FLOATS	ID_DET_ENDS	VBUS_DET_ENDS	-
				15	14	13	12	11	10	9	8
				-	-	-	-	-	-	-	-
				7	6	5	4	3	2	1	0
				-	-	USBOVPS	-	USBDETS	-	-	-
3	Interrupt Status 1 Table 108	W1C	h00_00_00	23	22	21	20	19	18	17	16
				-	-	-	GPIOLV3I	GPIOLV2I	GPIOLV1I	GPIOLV0I	SCPI
				15	14	13	12	11	10	9	8
				CLKI	THERM130	THERM125	THERM120	THERM110	MEMHLDI	WARMI	PCI
				7	6	5	4	3	2	1	0
				RTCRSTI	SYSRSTI	WDIRESTI	PWRON2I	PWRON1I	-	TODAI	1HZI
4	Interrupt Mask 1 Table 109	R/W	h5F_77_FB	23	22	21	20	19	18	17	16
				-	-	-	GPIOLV3M	GPIOLV2M	GPIOLV1M	GPIOLV0M	SCPM
				15	14	13	12	11	10	9	8
				CLKM	THERM130M	THERM125M	THERM120M	THERM110M	MEMHLDM	WARMM	PCM
				7	6	5	4	3	2	1	0
				RTCRSTM	SYSRSTM	WDIRESTM	PWRON2M	PWRON1M	-	TODAM	1HZM

Table 104. SPI/I²C Register Map

5	Interrupt Sense 1 Table 110	RO	hXX_XX_XX	23	22	21	20	19	18	17	16
				-	-	-	GPIOLV3S	GPIOLV2S	GPIOLV1S	GPIOLV0S	-
				15	14	13	12	11	10	9	8
				CLKS	THERM130S	THERM125S	THERM120S	THERM110S	-	-	-
				7	6	5	4	3	2	1	0
				-	-	-	PWRON2S	PWRON1S	-	-	-
6	Power Up Mode Sense Table 111	RO	h00_00_XX	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	-	-	-	-	-
				7	6	5	4	3	2	1	0
				-	-	PUMS5S	PUMS4S	PUMS3S	PUMS2S	PUMS1S	ICTESTS
7	Identification Table 112	RW	h00_00_08	23	22	21	20	19	18	17	16
				PAGE[4:0]					-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	-	FAB[2:0]			FIN[2]
				7	6	5	4	3	2	1	0
				FIN[1:0]		FULL_LAYER_REV[2:0]			METAL_LAYER_REV[2:0]		
8	Regulator Fault Sense Table 113	RW	h00_XX_XX	23	22	21	20	19	18	17	16
				REGSCPEN	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	VGEN2FAULT	VGEN1FAULT	VDACFAULT	VUSB2FAULT	VUSBFAULT
				7	6	5	4	3	2	1	0
				SWBSTFAULT	SW5FAULT	SW4BFAULT	SW4AFAULT	SW3FAULT	SW2FAULT	RSVD	SW1FAULT
9-11	Reserved	NU	hXX_XX_XX	23	22	21	20	19	18	17	16
				-							
				15	14	13	12	11	10	9	8
				-							
				7	6	5	4	3	2	1	0
				-	-		-	-	-	-	-
12	Unused	NU	h00_00_00	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	-	-	-	-	-
				7	6	5	4	3	2	1	0
				-	-	-	-	-	-	-	-
13	Power Control 0 Table 118	R/W	h00_00_40	23	22	21	20	19	18	17	16
				COINCHEN	VCOIN[2:0]				-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	-	-	-	PCUTEXPB	-
				7	6	5	4	3	2	1	0
				-	CLK32KMCUEN	USEROFFCLK	DRM	USEROFFSPI	WARMEN	PCCOUNTEN	PCEN
14	Power Control 1 Table 119	R/W	h00_00_00	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				PCMAXCNT[3:0]				PCCOUNT[3:0]			
				7	6	5	4	3	2	1	0
				PCT[7:0]							

Table 104. SPI/I²C Register Map

15	Power Control 2 Table 120	R/W	h40_03_00	23	22	21	20	19	18	17	16
				STBYDLY[1:0]		ON_STBY_LP	-	-	CLKDRV[1:0]		-
				15	14	13	12	11	10	9	8
				-	SPIDRV[1:0]		WDIRESET	-	STANDBYINV	GLBRSTTMR[1:0]	
				7	6	5	4	3	2	1	0
				PWRON2DBNC[1:0]		PWRON1BDBNC[1:0]		-	PWRON2 RSTEN	PWRON1RSTEN	RESTARTEN
16	Memory A Table 121	R/W	h00_00_00	23	22	21	20	19	18	17	16
				MEMA[23:16]							
				15	14	13	12	11	10	9	8
				MEMA[15:8]							
				7	6	5	4	3	2	1	0
				MEMA[7:0]							
17	Memory B Table 122	R/W	h00_00_00	23	22	21	20	19	18	17	16
				MEMB[23:16]							
				15	14	13	12	11	10	9	8
				MEMB[15:8]							
				7	6	5	4	3	2	1	0
				MEMB[7:0]							
18	Memory C Table 123	R/W	h00_00_00	23	22	21	20	19	18	17	16
				MEMC[23:16]							
				15	14	13	12	11	10	9	8
				MEMC[15:8]							
				7	6	5	4	3	2	1	0
				MEMC[7:0]							
19	Memory D Table 124	R/W	h00_00_00	23	22	21	20	19	18	17	16
				MEMD[23:16]							
				15	14	13	12	11	10	9	8
				MEMD[15:8]							
				7	6	5	4	3	2	1	0
				MEMD[7:0]							
20	RTC Time Table 125	R/W	h00_00_00	23	22	21	20	19	18	17	16
				RTCCALMODE[1:0]		RTCCAL[4:0]					TOD[16]
				15	14	13	12	11	10	9	8
				TOD[15:8]							
				7	6	5	4	3	2	1	0
				TOD[7:0]							
21	RTC Alarm Table 126	R/W	h01_FF_FF	23	22	21	20	19	18	17	16
				RTCDIS	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	TODA[16]
				15	14	13	12	11	10	9	8
				TODA[15:8]							
				7	6	5	4	3	2	1	0
				TODA[7:0]							
22	RTC Day Table 127	R/W	h00_00_00	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	DAY[14:8]						
				7	6	5	4	3	2	1	0
				DAY[7:0]							

Table 104. SPI/I²C Register Map

23	RTC Day Alarm Table 128	R/W	h00_7F_FF	23	22	21	20	19	18	17	16				
				-	-	-	-	-	-	-	-				
				15	14	13	12	11	10	9	8				
				-	DAYA[14:8]										
				7	6	5	4	3	2	1	0				
				DAYA[7:0]											
24	Regulator 1A/B Voltage Table 129	R/WM	hXX_XX_XX	23	22	21	20	19	18	17	16				
				RSVD[5:0]						RSVD[5:4]					
				15	14	13	12	11	10	9	8				
				RSVD[3:0]				SW1ASTBY[5:2]							
				7	6	5	4	3	2	1	0				
				SW1ASTBY[1:0]		SW1A[5:0]									
25	Regulator 2&3 Voltage Table 130	R/WM	hXX_XX_XX	23	22	21	20	19	18	17	16				
				-	SW3STBY[4:0]					-	SW3[4]				
				15	14	13	12	11	10	9	8				
				SW3[3:0]				SW2STBY[5:2]							
				7	6	5	4	3	2	1	0				
				SW2STBY[1:0]		SW2[5:0]									
26	Regulator 4 Voltage Table 131	R/WM	hXX_XX_XX	23	22	21	20	19	18	17	16				
				SW4BHI[1:0]		SW4BSTBY[4:0]					SW4B[4]				
				15	14	13	12	11	10	9	8				
				SW4B[3:0]				SW4AHI[1:0]		SW4ASTBY[4:3]					
				7	6	5	4	3	2	1	0				
				SW4ASTBY[2:0]			SW4A[4:0]								
27	Regulator 5 Voltage Table 132	R/WM	h00_XX_XX	23	22	21	20	19	18	17	16				
				-	-	-	-	-	-	-	-				
				15	14	13	12	11	10	9	8				
				-	SW5TBY[4:0]					-	-				
				7	6	5	4	3	2	1	0				
				-	-	-	SW5[4:0]								
28	Regulator 1, 2 Mode Table 133	R/W	hEX_XX_8X	23	22	21	20	19	18	17	16				
				PLLX	PLLEN	SW2DVSSPEED[1:0]		SW2UOMODE	SW2MHMODE	SW2MODE[3:2]					
				15	14	13	12	11	10	9	8				
				SW2MODE[1:0]		-	-	-	-	-	-				
				7	6	5	4	3	2	1	0				
				SW1DVSSPEED[1:0]		SW1AUOMODE	SW1AMHMODE	SW1AMODE[3:0]							
29	Regulator 3, 4, 5 Mode Table 134	R/W	hXX_XX_XX	23	22	21	20	19	18	17	16				
				SW5UOMODE	SW5MHMODE	SW5MODE[3:0]				SW4BUOMODE	SW4BMHMODE				
				15	14	13	12	11	10	9	8				
				SW4BMODE[3:0]				SW4AUOMODE	SW4AMHMODE	SW4AMODE[3:2]					
				7	6	5	4	3	2	1	0				
				SW4AMODE[1:0]		SW3UOMODE	SW3MHMODE	SW3MODE[3:0]							
30	Regulator Setting 0 Table 135	R/WM	h00_XX_XX	23	22	21	20	19	18	17	16				
				-	-	-	-	-	-	-	-				
				15	14	13	12	11	10	9	8				
				-	-	-	VUSB2[1:0]		VPLL[1:0]		VGEN2[2]				
				7	6	5	4	3	2	1	0				
				VGEN2[1:0]		VDAC[1:0]		-	VGEN1[2:0]						

Table 104. SPI/I²C Register Map

31	SWBST Control Table 136	R/WM	h00_00_XX	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	-	-	-	-	-
				7	6	5	4	3	2	1	0
				SPARE	SWBSTSTBYMODE[1:0]		SPARE	SWBSTMODE[1:0]		SWBST[1:0]	
32	Regulator Mode 0 Table 137	R/WM	h0X_XX_XX	23	22	21	20	19	18	17	16
				-	-	-	VUSB2MODE	VUSB2STBY	VUSB2EN	VUSB2CONFIG	VPLLSTBY
				15	14	13	12	11	10	9	8
				VPLLEN	VGEN2MODE	VGEN2STBY	VGEN2EN	VGEN2CONFIG	VREFDDREN	-	-
				7	6	5	4	3	2	1	0
				RSVD	VDACMODE	VDACSTBY	VDACEN	VUSBEN	VUSBSEL	VGEN1STBY	VGEN1EN
33	GPIOLV0 Control Table 138	R/W	h00_18_0A	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	SPARE
				15	14	13	12	11	10	9	8
				SRE1	SRE0	PUS1	PUS0	PUE	DSE	ODE	PKE
				7	6	5	4	3	2	1	0
				INT1	INT0	DBNC1	DBNC0	HYS	DOUT	DIN	DIR
34	GPIOLV1 Control Table 139	R/W	h00_18_0A	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	SPARE
				15	14	13	12	11	10	9	8
				SRE1	SRE0	PUS1	PUS0	PUE	DSE	ODE	PKE
				7	6	5	4	3	2	1	0
				INT1	INT0	DBNC1	DBNC0	HYS	DOUT	DIN	DIR
35	GPIOLV2 Control Table 140	R/W	h00_18_0A	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	SPARE
				15	14	13	12	11	10	9	8
				SRE1	SRE0	PUS1	PUS0	PUE	DSE	ODE	PKE
				7	6	5	4	3	2	1	0
				INT1	INT0	DBNC1	DBNC0	HYS	DOUT	DIN	DIR
36	GPIOLV3 Control Table 141	R/W	h00_18_0A	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	SPARE
				15	14	13	12	11	10	9	8
				SRE1	SRE0	PUS1	PUS0	PUE	DSE	ODE	PKE
				7	6	5	4	3	2	1	0
				INT1	INT0	DBNC1	DBNC0	HYS	DOUT	DIN	DIR
37	USB Timing Table 142	R/W	hXX_XX_XX	23	22	21	20	19	18	17	16
				READVALID	-	-	-	TD[3:0]			
				15	14	13	12	11	10	9	8
				SWITCHING_WAIT[3:0]				Long_KEY_PRESS[3:0]			
				7	6	5	4	3	2	1	0
				KEY_PRESS[3:0]				DEVICE_WAKE_UP[3:0]			
38	USB Button Table 143	R/C	hXX_XX_XX	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	UNKNOWN	Error	S12	S11	S10	S9	S8
				7	6	5	4	3	2	1	0
				S7	S6	S5	S4	S3	S2	S1	S0

Table 104. SPI/I²C Register Map

39	USB control Table 144	R/W	hXX_XX_XX	23	22	21	20	19	18	17	16
				READVALID	DM_SWITCHING[2:0]			DP_SWITCHING[2:0]			VBUS_SWITCHING[1]
				15	14	13	12	11	10	9	8
				VBUS_SWITCHING[0]	-		SW_HOLD	-	-	VOTGEN	CLK_RST
				7	6	5	4	3	2	1	0
				ACTIVE	RST	TTY_SPKL	RESET	SWITCH_OPEN	RAWDATA	MANUAL_SW_B	WAIT
40	USB Device Type Table 145	R	hXX_XX_XX	23	22	21	20	19	18	17	16
				USB_ADC_ID_RESULTS[4:0]					-	UKN_DEVICE	ID_FACTORY
				15	14	13	12	11	10	9	8
				UARTJIG2	UARTJIG1	USBJIG2	USBJIG1	AVCHRG	A/V	TTY	PPD
				7	6	5	4	3	2	1	0
				USB OTG	DEDICATED_CHG	USB CHG	5W CHG	UART	USB	AUDIO_TYPE_2	AUDIO_TYPE_1
41 to 42	Unused	NU	h00_00_00	23	22	21	20	19	18	17	16
				-	-	-	-	-	-	-	-
				15	14	13	12	11	10	9	8
				-	-	-	-	-	-	-	-
				7	6	5	4	3	2	1	0
				-	-	-	-	-	-	-	-
43	ADC 0 Table 147	R/W	h00_00_00	23	22	21	20	19	18	17	16
				SPARE	SPARE	SPARE	TSPENDETEN	SPARE	TSSTOP[2:0]		
				15	14	13	12	11	10	9	8
				TSHOLD	TSCONT	TSSTART	TSEN	SPARE	SPARE	DIETEMP_EN	THERM
				7	6	5	4	3	2	1	0
				SPARE	ADSTOP[2:0]			ADHOLD	ADCONT	ADSTART	ADEN
44	ADC 1 Table 148	R/W	h00_00_00	23	22	21	20	19	18	17	16
				TSDLY3[3:0]				TSDLY2[3:0]			
				15	14	13	12	11	10	9	8
				TSDLY1[3:0]				ADDLY3[3:0]			
				7	6	5	4	3	2	1	0
				ADDLY2[3:0]				ADDLY1[3:0]			
45	ADC 2 Table 149	R/W	h00_00_00	23	22	21	20	19	18	17	16
				ADSEL5[3:0]				ADSEL4[3:0]			
				15	14	13	12	11	10	9	8
				ADSEL3[3:0]				ADSEL2[3:0]			
				7	6	5	4	3	2	1	0
				ADSEL1[3:0]				ADSEL0[3:0]			
46	ADC 3 Table 150	R/W	h00_00_00	23	22	21	20	19	18	17	16
				TSSEL7[1:0]		TSSEL6[1:0]		TSSEL5[1:0]		TSSEL4[1:0]	
				15	14	13	12	11	10	9	8
				TSSEL3[1:0]		TSSEL2[1:0]		TSSEL1[1:0]		TSSEL0[1:0]	
				7	6	5	4	3	2	1	0
				ADSEL7[3:0]				ADSEL6[3:0]			

Table 104. SPI/I²C Register Map

47	ADC 4 Table 151	R/W	h00_00_00	23	22	21	20	19	18	17	16
				ADRESULT1[9:2]							
				15	14	13	12	11	10	9	8
				ADRESULT1[1:0]		-	-	ADRESULT0[9:6]			
				7	6	5	4	3	2	1	0
				ADRESULT0[5:0]						-	-
48	ADC 5 Table 152	R/W	h00_00_00	23	22	21	20	19	18	17	16
				ADRESULT3[9:2]							
				15	14	13	12	11	10	9	8
				ADRESULT3[1:0]		-	-	ADRESULT2[9:6]			
				7	6	5	4	3	2	1	0
				ADRESULT2[5:0]						-	-
49	ADC 6 Table 153	R/W	h00_00_00	23	22	21	20	19	18	17	16
				ADRESULT5[9:2]							
				15	14	13	12	11	10	9	8
				ADRESULT5[1:0]		-	-	ADRESULT4[9:6]			
				7	6	5	4	3	2	1	0
				ADRESULT4[5:0]						-	-
50	ADC 7 Table 154	R/W	h00_00_00	23	22	21	20	19	18	17	16
				ADRESULT7[9:2]							
				15	14	13	12	11	10	9	8
				ADRESULT7[9:2]		-	-	ADRESULT6[9:6]			
				7	6	5	4	3	2	1	0
				ADRESULT6[5:0]						-	-
51	Input Monitoring Table 155	R/W	h01_31_7E	23	22	21	20	19	18	17	16
				-	-		-		-		
				15	14	13	12	11	10	9	8
				-				-			
				7	6	5	4	3	2	1	0
				-		LOWBATT[1:0]		CHREN	-	-	
52	Supply Debounce Table 156	R/W	h00_03_FD	23	22	21	20	19	18	17	16
				-	-	-	-	-		DIE_TEMP_DB[1:0]	
				15	14	13	12	11	10	9	8
				SUP_OVP_DB[1:0]		-			CHRGLED OVRD	-	
				7	6	5	4	3	2	1	0
				-		VBUSDB[1:0]		VBATTDB[1:0]		-	
53	VBUS monitoring Table 157	R/W	hC0_36_1B	23	22	21	20	19	18	17	16
				-	-	-				-	
				15	14	13	12	11	10	9	8
				-	-			-			-
				7	6	5	4	3	2	1	0
				-		VBUSTH[2:0]			VBUSTL[2:0]		

Table 104. SPI/I²C Register Map

54	LED Control Table 158	R/W	h60_06_00	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
				CHRGLEDGEN	CHRGLEDG[1:0]		CHRGLEDGDC[5:1]				
				15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
				CHRGLEDGDC[0]	CHRGLEDG RAMP	LEDGPER[1:0]		CHRGLEDREN	CHRGLEDR[1:0]		CHRGLEDRDC[5]
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
				CHRGLEDRDC[4:0]					CHRGLEDR RAMP	CHRGLEDRPER[1:0]	
55	PWM Control Table 159	R/W	h00_00_00	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
				PWM2CLKDIV[5:0]						PWM2DUTY[5:4]	
				15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
				PWM2DUTY[3:0]				PWM1CLKDIV[5:2]			
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
				PWM1CLKDIV[1:0]		PWM1DUTY[5:0]					
56 to 63	Unused	NU	h00_00_00	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
				-	-	-	-	-	-	-	-
				15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
				-	-	-	-	-	-	-	-
				7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
				-	-	-	-	-	-	-	-

7.10.4 SPI Register's Bit Description

Table 105. Register 0, Interrupt Status 0

Name	Bit #	R/W	Reset	Default	Description
ADCDONEI	0	RW1C	RESETB	0x0	ADC has finished requested conversions
TSDONEI	1	RW1C	RESETB	0x0	Touchscreen has finished requested conversions
TSPENDET	2	RW1C	RESETB	0x0	Touch screen pen detection
USBDET	3	RW1C	OFFB	0x0	USB detect
Reserved	4	RW1C	NONE	0x0	Reserved
USBOVP	5	RW1C	RESETB	0x0	USB over voltage protection
Reserved	12:6	RW1C	NONE	0x0	Reserved
LOWBATT	13	RW1C	RESETB	0x0	Low battery threshold warning
Reserved	14	RW1C	NONE	0x0	Reserved
ATTACH	15	RW1C	MUSBRSTB	0x0	1: accessory attached
DETACH	16	RW1C	MUSBRSTB	0x0	1: accessory detached
KP	17	RW1C	MUSBRSTB	0x0	1: remote controller key is pressed
LKP	18	RW1C	MUSBRSTB	0x0	1: remote controller long key is pressed
LKR	19	RW1C	MUSBRSTB	0x0	1: remote controller long key is released
UNKNOWN_ATTA	20	RW1C	MUSBRSTB	0x0	1: an unknown accessory is attached
ADC_CHANGE	21	RW1C	MUSBRSTB	0x0	1: ADC Result has changed when the RAW DATA = 0
STUCK_KEY	22	RW1C	MUSBRSTB	0x0	1: Stuck key is detected
STUCK_KEY_RCV	23	RW1C	MUSBRSTB	0x0	1: Stuck key is recovered

Table 106. Interrupt Mask 0

Name	Bit #	R/W	Reset	Default	Description
ADCDONEM	0	R/W	RESETB	0x1	ADCDONEI mask bit
TSDONEM	1	R/W	RESETB	0x1	TSDONEI mask bit
TSPENDETM	2	R/W	RESETB	0x1	Touch screen pen detect mask bit
USBDETM	3	R/W	OFFB	0x1	USBDET mask bit
Reserved	4	R/W	NONE	0x0	Reserved
USBOVPM	5	R/W	RESETB	0x0	USB over voltage protection
Reserved	12:6	R/W	NONE	0x0	Reserved
LOWBATTM	13	R/W	RESETB	0x1	LOBATLI mask bit
Reserved	14	RW1C	NONE	0x0	Reserved
ATTACH_M	15	R/W	RESETB	0x1	DETACH mask bit
DETACH_M	16	R/W	RESETB	0x1	KP mask bit
KP_M	17	R/W	RESETB	0x1	LKP mask bit
LKP_M	18	R/W	RESETB	0x1	LKR mask bit
LKR_M	19	R/W	RESETB	0x1	DETACH mask bit
UKNOWN_ATTA_M	20	R/W	RESETB	0x1	UNKNOWN_ATTA mask bit

Table 106. Interrupt Mask 0

Name	Bit #	R/W	Reset	Default	Description
ADC_CHANGE_M	21	R/W	RESETB	0x1	VBUS power supply type identification completed mask
STUCK_KEY_M	22	R/W	RESETB	0x1	ID resistance detection finished mask
STUCK_KEY_RCV_M	23	R/W	RESETB	0x1	For future use

Table 107. Register 2, Interrupt Sense 0

Name	Bit #	R/W	Reset	Default	Description
Unused	2-0	R		0x0	Not available
USBDETS	3	R	NONE	S	USBDET sense bit
Reserved	4	R	NONE	0x0	Reserved
USBOVPS	5	R	NONE	S	USBOVP sense bit
Reserved	6	R	NONE	0x0	Reserved
Unused	7	R	NONE	0x0	Not available
Reserved	9:8	R	NONE	0x0	Reserved
Unused	16-10	R		0x0	Not available
VBUS_DET_ENDS	17	R	MUSBRSTB	0x0	VBUS power supply type identification completed sense bit
ID_DET_ENDS	18	R	MUSBRSTB	0x0	ID resistance detection finished sense bit
ID_FLOATS	19	R	NONE	S	ID float sense bit
ID_GNDS	20	R	MUSBRSTB	0x0	ID ground sense bit 0: no 1: yes
MUSB_ADC_STATUS	21	R	NONE	X	Mini USB ADC conversion status 1: ADC conversion completed 0: ADC conversion in progress
Unused	23-22	R		0x0	Not available

Table 108. Register 3, Interrupt Status 1

Name	Bit #	R/W	Reset	Default	Description
1HZI	0	RW1C	RTCPORB	0x0	1.0 Hz time tick
TODAI	1	RW1C	RTCPORB	0x0	Time of day alarm
Unused	2	R		0x0	Not available
PWRON1I	3	RW1C	OFFB	0x0	PWRON1 event
PWRON2I	4	RW1C	OFFB	0x0	PWRON2 event
WDIRESETI	5	RW1C	RTCPORB	0x0	WDI system reset event
SYSRSTI	6	RW1C	RTCPORB	0x0	PWRON system reset event
RTCRSTI	7	RW1C	RTCPORB	0x1	RTC reset event
PCI	8	RW1C	OFFB	0x0	Power cut event
WARMI	9	RW1C	RTCPORB	0x0	Warm start event
MEMHLDI	10	RW1C	RTCPORB	0x0	Memory hold event
THERM110	11	RW1C	RESETB	0x0	110 °C thermal threshold

Table 108. Register 3, Interrupt Status 1

Name	Bit #	R/W	Reset	Default	Description
THERM120	12	RW1C	RESETB	0x0	120 °C thermal threshold
THERM125	13	RW1C	RESETB	0x0	125 °C thermal threshold
THERM130	14	RW1C	RESETB	0x0	130 °C thermal threshold
CLKI	15	RW1C	RESETB	0x0	Clock source change
SCPI	16	RW1C	RESETB	0x0	Short-circuit protection trip detection
GPIOLV1I	17	RW1C	RESETB	0x0	GPIOLV1 interrupt
GPIOLV2I	18	RW1C	RESETB	0x0	GPIOLV2 interrupt
GPIOLV3I	19	RW1C	RESETB	0x0	GPIOLV3 interrupt
GPIOLV4I	20	RW1C	RESETB	0x0	GPIOLV4 interrupt
Unused	21	R		0x0	Not available
Reserved	22	R	NONE	0x0	Reserved
Unused	23	R	RESETB	0x0	Not available

Table 109. Register 4, Interrupt Mask 1

Name	Bit #	R/W	Reset	Default	Description
1HZM	0	R/W	RTCPORB	0x1	1HZI mask bit
TODAM	1	R/W	RTCPORB	0x1	TODAI mask bit
Unused	2	R		0x1	Not available
PWRON1M	3	R/W	OFFB	0x1	PWRON1 mask bit
PWRON2M	4	R/W	OFFB	0x1	PWRON2 mask bit
WDIRESETM	5	R/W	RTCPORB	0x1	WDIRESETI mask bit
SYSRSTM	6	R/W	RTCPORB	0x1	SYSRSTI mask bit
RTCRSTM	7	R/W	RTCPORB	0x1	RTCRSTI mask bit
PCM	8	R/W	OFFB	0x1	PCI mask bit
WARMM	9	R/W	RTCPORB	0x1	WARMI mask bit
MEMHLDM	10	R/W	RTCPORB	0x1	MEMHLDI mask bit
THERM110M	11	R/W	RESETB	0x1	THERM110 mask bit
THERM120M	12	R/W	RESETB	0x1	THERM120 mask bit
THERM125M	13	R/W	RESETB	0x1	THERM125 mask bit
THERM130M	14	R/W	RESETB	0x1	THERM130 mask bit
CLKM	15	R/W	RESETB	0x1	CLKI mask bit
SCPM	16	R/W	RESETB	0x1	Short-circuit protection trip mask bit
GPIOLV1M	17	R/W	RESETB	0x1	GPIOLV1 interrupt mask bit
GPIOLV2M	18	R/W	RESETB	0x1	GPIOLV2 interrupt mask bit
GPIOLV3M	19	R/W	RESETB	0x1	GPIOLV3 interrupt mask bit
GPIOLV4M	20	R/W	RESETB	0x1	GPIOLV4 interrupt mask bit
Unused	21	R		0x0	Not available

Table 109. Register 4, Interrupt Mask 1

Name	Bit #	R/W	Reset	Default	Description
Reserved	22	R	NONE	0x0	Reserved
Unused	23	R		0x1	Not available

Table 110. Register 5, Interrupt Sense 1

Name	Bit #	R/W	Reset	Default	Description
Unused	2-0	R		0x0	Not available
PWRON1S	3	R	NONE	S	PWRON1I sense bit
PWRON2S	4	R	NONE	S	PWRON2I sense bit
Unused	10-5	R		0x0	Not available
THERM110S	11	R	NONE	S	THERM110 sense bit
THERM120S	12	R	NONE	S	THERM120 sense bit
THERM125S	13	R	NONE	S	THERM125 sense bit
THERM130S	14	R	NONE	S	THERM130 sense bit
CLKS	15	R	NONE	0x0	CLKI sense bit
Unused	21-16	R		0x00	Not available
Reserved	22	R	NONE	0x0	Reserved
Unused	23	R	NONE	0x0	Not available

Table 111. Register 6, Power Up Mode Sense

Name	Bit #	R/W	Reset	Default (76)	Description
ICTESTS	0	R	NONE	S	ICTEST sense state
PUMS1S	1	R	NONE	L	PUMS1 state
PUMS2S	2	R	NONE	L	PUMS2 state
PUMS3S	3	R	NONE	L	PUMS3 state
PUMS4S	4	R	NONE	L	PUMS4 state
PUMS5S	5	R	NONE	L	PUMS5 state
Unused	8-6	R		0x0	Not available
Reserved	9	R	NONE	0x0	Reserved
Unused	23-10	R		0x0000	Not available

76. L = Loaded PUMSx level at startup.

Table 112. Register 7, Identification

Name	Bit #	R/W	Reset	Default	Description
METAL_LAYER_REV[2:0]	2-0	R	NONE	X	Metal Layer version Pass 2.4 =100
FULL_LAYER_REV[2:0]	5-3	R	NONE	X	Full Layer version Pass 2.4 = 010
FIN[2:0]	8-6	R	NONE	X	FIN version Pass 2.4 = 000

Table 112. Register 7, Identification

Name	Bit #	R/W	Reset	Default	Description
FAB[2:0]	11-9	R	NONE	X	FAB version Pass 2.4 = 000
Unused	18-12	R		0x0	Not available
PAGE[4:0]	23-19	R/W	DIGRESETB	0x0	SPI Page

Table 113. Register 8, Regulator Fault Sense

Name	Bit #	R/W	Reset	Default	Description
SW1FAULT	0	R	NONE	S	SW1 fault detection
Reserved	1	R	NONE	0x0	Reserved
SW2FAULT	2	R	NONE	S	SW2 fault detection
SW3FAULT	3	R	NONE	S	SW3 fault detection
SW4AFAULT	4	R	NONE	S	SW4A fault detection
SW4BFAULT	5	R	NONE	S	SW4B fault detection
SW5FAULT	6	R	NONE	S	SW5 fault detection
SWBSTFAULT	7	R	NONE	S	SWBST fault detection
VUSBFAULT	8	R	NONE	S	VUSB fault detection
VUSB2FAULT	9	R	NONE	S	VUSB2 fault detection
VDACFAULT	10	R	NONE	S	VDAC fault detection
VGEN1FAULT	11	R	NONE	S	VGEN1 fault detection
VGEN2FAULT	12	R	NONE	S	VGEN2 fault detection
Unused	22-13	R		0x00	Not available
REGSCPEN	23	R/W	RESETB	0x0	Regulator short-circuit protect enable

Table 114. Register 9, Reserved

Name	Bit #	R/W	Reset	Default	Description
Reserved	1-23	R	NONE	0x000020	Reserved

Table 115. Register 10, Reserved

Name	Bit #	R/W	Reset	Default	Description
Reserved	1-23	R	NONE	0x00013A	Reserved

Table 116. Register 11, Reserved

Name	Bit #	R/W	Reset	Default	Description
Reserved	1-23	R	NONE	0x000000	Reserved

Table 117. Register 12, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	23-0	R		0x000000	Not available

Table 118. Register 13, Power Control 0

Name	Bit #	R/W	Reset	Default	Description
PCEN	0	R/W	RTCPORB	0x0	Power cut enable
PCCOUNTEN	1	R/W	RTCPORB	0x0	Power cut counter enable
WARMEN	2	R/W	RTCPORB	0x0	Warm start enable
USEROFFSPI	3	R/W	RESETB	0x0	SPI command for entering user off modes
DRM	4	R/W	RTCPORB (77)	0x0	Keeps VSRTC and CLK32KMCU on for all states
USEROFFCLK	5	R/W	RTCPORB	0x0	Keeps the CLK32KMCU active during user off
CLK32KMCUEN	6	R/W	RTCPORB	0x1	Enables the CLK32KMCU
Unused	8-7	R		0x00	Not available
PCUTEXPB	9	R/W	RTCPORB	0x0	PCUTEXPB=1 at a startup event indicates the PCUT timer did not expire (assuming it was set to 1 after booting)
Unused	18-10	R		0x000	Not available
Reserved	19	R	NONE	0x0	Reserved
VCOIN[2:0]	22-20	R/W	RTCPORB	0x00	Coin cell charger voltage setting
COINCHEN	23	R/W	RTCPORB	0x0	Coin cell charger enable

Notes:
77. Reset by RTCPORB but not during a GLBRST (global reset)

Table 119. Register 14, Power Control 1

Name	Bit #	R/W	Reset	Default	Description
PCT[7:0]	7-0	R/W	RTCPORB	0x00	Power cut timer
PCCOUNT[3:0]	11-8	R/W	RTCPORB	0x00	Power cut counter
PCMAXCNT[3:0]	15-12	R/W	RTCPORB	0x00	Maximum allowed number of power cuts
Unused	23-16	R		0x00	Not available

Table 120. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description
RESTARTEN	0	R/W	RTCPORB	0x0	Enables automatic restart after a system reset
PWRON1RSTEN	1	R/W	RTCPORB	0x0	Enables system reset on PWRON1 pin
PWRON2RSTEN	2	R/W	RTCPORB	0x0	Enables system reset on PWRON2 pin
Unused	3	R		0x0	Not available
PWRON1DBNC[1:0]	5-4	R/W	RTCPORB	0x00	Sets debounce time on PWRON1 pin
PWRON2DBNC[1:0]	7-6	R/W	RTCPORB	0x00	Sets debounce time on PWRON2 pin
GLBRSTTMR[1:0]	9-8	R/W	RTCPORB	0x01	Sets Global reset time
STANDBYINV	10	R/W	RTCPORB	0x0	If set then STANDBY is interpreted as active low
Unused	11	R		0x0	Not available
WDIRESET	12	R/W	RESETB	0x0	Enables system reset through WDI
SPIDRV[1:0]	14-13	R/W	RTCPORB	0x01	SPI drive strength
Unused	16-15	R		0x00	Not available

Table 120. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description
CLK32KDRV[1:0]	18-17	R/W	RTCPORB	0x01	CLK32K and CLK32KMCU drive strength (master control bits)
Unused	20-19	R		0x00	Not available
ON_STBY_LP	21	R/W	RESETB	0x0	On Standby Low Power Mode 0 = Low power mode disabled 1 =Low power mode enabled
STBYDLY[1:0]	23-22	R/W	RESETB	0x01	Standby delay control

Table 121. Register 16, Memory A

Name	Bit #	R/W	Reset	Default	Description
MEMA[23:0]	23-0	R/W	RTCPORB	0x000000	Backup memory A

Table 122. Register 17, Memory B

Name	Bit #	R/W	Reset	Default	Description
MEMB[23:0]	23:0	R/W	RTCPORB	0x000000	Backup memory B

Table 123. Register 18, Memory C

Name	Bit #	R/W	Reset	Default	Description
MEMC[23:0]	23-0	R/W	RTCPORB	0x000000	Backup memory C

Table 124. Register 19, Memory D

Name	Bit #	R/W	Reset	Default	Description
MEMD[23:0]	23-0	R/W	RTCPORB	0x000000	Backup memory D

Table 125. Register 20, RTC Time

Name	Bit #	R/W	Reset	Default	Description
TOD[16:0]	16-0	R/W	RTCPORB (78)	0x00000	Time of day counter
RTCCAL[4:0]	21-17	R/W	RTCPORB (78)	0x00	RTC calibration count
RTCCALMODE[1:0]	23-22	R/W	RTCPORB (78)	0x0	RTC calibration mode

Notes
78. Reset by RTCPORB but not during a GLBRST (global reset)

Table 126. Register 21, RTC Alarm

Name	Bit #	R/W	Reset	Default	Description
TODA[16:0]	16-0	R/W	RTCPORB (79)	0x1FFFF	Time of day alarm
Unused	22-17	R		0x00	Not available
RTCDIS	23	R/W	RTCPORB (79)	0x0	Disable RTC

Notes
79. Reset by RTCPORB but not during a GLBRST (global reset)

Table 127. Register 22, RTC Day

Name	Bit #	R/W	Reset	Default	Description
DAY[14:0]	14-0	R/W	RTCPORB (80)	0x0000	Day counter
Unused	23-15	R		0x000	Not available

Notes
80. Reset by RTCPORB but not during a GLBRST (global reset)

Table 128. Register 23, RTC Day Alarm

Name	Bit #	R/W	Reset	Default	Description
DAYA[14:0]	14-0	R/W	RTCPORB (81)	0x7FFF	Day alarm
Unused	23-15	R		0x000	Not available

Notes
81. Reset by RTCPORB but not during a GLBRST (global reset)

Table 129. Register 24, Regulator 1A/B Voltage

Name	Bit #	R/W	Reset	Default	Description
SW1A[5:0]	5-0	R/WM	NONE	*	SW1 setting in normal mode
SW1ASTBY[5:0]	11-6	R/WM	NONE	*	SW1 setting in Standby mode
Reserved	23-12	R	NONE	*	Not available

Table 130. Register 25, Regulator 2 & 3 Voltage

Name	Bit #	R/W	Reset	Default	Description
SW2[5:0]	5-0	R/WM	NONE	*	SW2 setting in normal mode
SW2STBY[5:0]	11-6	R/WM	NONE	*	SW2 setting in Standby mode
SW3[4:0]	16-12	R/WM	NONE	*	SW3 setting in normal mode
Unused	17	R		0x0	Not available
SW3STBY[4:0]	22-18	R/WM	NONE	*	SW3 setting in standby mode
Unused	23	R		0x0	Not available

Table 131. Register 26, Regulator 4A/B

Name	Bit #	R/W	Reset	Default	Description
SW4A[0:4]	4-0	R/WM	NONE	*	SW4A setting in normal mode
SW4ASTBY[4:0]	9-5	R/WM	NONE	*	SW4A setting in Standby mode
SW4AHI[1:0]	11-10	R/WM	NONE	*	SW4A high setting
SW4B[4:0]	16-12	R/WM	NONE	*	SW4B setting in normal mode
SW4BSTBY[4:0]	21-17	R/WM	RESETB	*	SW4B setting in Standby mode
SW4BHI[1:0]	23-22	R/WM	RESETB	*	SW4B high setting

Table 132. Register 27, Regulator 5 Voltage

Name	Bit #	R/W	Reset	Default	Description
SW5[4:0]	4-0	R/WM	NONE	*	SW4 setting in normal mode
Unused	9-5	R		*	Not available
SW5STBY[4:0]	14-10	R/WM	NONE	*	SW5 setting in Standby mode
Unused	23-15	R		0x000	Not available

Table 133. Register 28, Regulators 1 & 2 Operating Mode

Name	Bit #	R/W	Reset	Default	Description
SW1AMODE[3:0]	3-0	R/W	RESETB	0xA	SW1A operating mode
SW1AMHMODE	4	R/W	OFFB	0x0	SW1A Memory Hold mode
SW1AUOMODE	5	R/W	OFFB	0x0	SW1A User Off mode
SW1DVSSPEED[1:0]	7-6	R/W	RESETB	0x1	SW1 DVS1 speed
Unused	13-8	R		0x00	Not available
SW2MODE[3:0](82)	17-14	R/W	RESETB	0xA	SW2 operating mode
SW2MHMODE	18	R/W	OFFB	0x0	SW2 Memory Hold mode
SW2UOMODE	19	R/W	OFFB	0x0	SW2 User Off mode
SW2DVSSPEED[1:0]	21-20	R/W	RESETB	0x01	SW2 DVS1 speed
PLLEN	22	R/W	RESETB	0x1	PLL enable
PLLX	23	R/W	RESETB	0x0	PLL multiplication factor

Notes

82. SWxMODE[3:0] bits will be reset to their default values by the startup sequencer, based on PUMS settings. An enabled switch will default to APS mode for both Normal and Standby operation.

Table 134. Register 29, Regulators 3, 4, and 5 Operating Mode

Name	Bit #	R/W	Reset	Default	Description
SW3MODE[3:0]	3-0	R/W	RESETB	0xA	SW3 operating mode
SW3MHMODE	4	R/W	OFFB	0x0	SW3 Memory Hold mode
SW3UOMODE	5	R/W	OFFB	0x0	SW3 User Off mode
SW4AMODE[3:0]	9-6	R/W	RESETB	0xA	SW4A operating mode
SW4AMHMODE	10	R/W	OFFB	0x0	SW4A Memory Hold mode
SW4AUOMODE	11	R/W	OFFB	0x0	SW4A User Off mode
SW4BMODE[3:0]	15-12	R/W	RESETB	0xA	SW4B operating mode
SW4BMHMODE	16	R/W	OFFB	0x0	SW4B Memory Hold mode
SW4BUOMODE	17	R/W	OFFB	0x0	SW4B User Off mode
SW5MODE[3:0](83)	21-18	R/W	RESETB	0xA	SW5 operating mode
SW5MHMODE	22	R/W	OFFB	0x0	SW5 Memory Hold mode
SW5UOMODE	23	R/W	OFFB	0x0	SW5 User Off mode

Notes

83. SWxMODE[3:0] bits will be reset to their default values by the startup sequencer, based on PUMS settings. An enabled regulator will default to APS mode for both Normal and Standby operation.

Table 135. Register 30, Regulator Setting 0

Name	Bit #	R/W	Reset	Default	Description
VGEN1[2:0]	2-0	R/WM	RESETB	*	VGEN1 setting
Unused	3	R		0x0	Not available
VDAC[1:0]	5-4	R/WM	RESETB	*	VDAC setting
VGEN2[2:0]	8-6	R/WM	RESETB	*	VGEN2 setting
VPLL[1:0]	10-9	R/WM	RESETB	*	VPLL setting
VUSB2[1:0]	12-11	R/WM	RESETB	*	VUSB2 setting
Unused	23-13	R		0x000	Not available

Table 136. Register 31, SWBST Control

Name	Bit #	R/W	Reset	Default	Description
SWBST[1:0]	1-0	R/W	NONE	*	SWBST setting
SWBSTMODE[1:0]	3-2	R/W	RESETB	0x2	SWBST mode
Spare	4	R/W	RESETB	0x0	Not available
SWBSTSTBYMODE[1:0]	6-5	R/W	RESETB	0x2	SWBST standby mode
Spare	7	R/W	RESETB	0x0	Not available
Unused	23-8	R		0x0000	Not available

Table 137. Register 32, Regulator Mode 0

Name	Bit #	R/W	Reset	Default	Description
VGEN1EN	0	R/W	NONE	*	VGEN1 enable
VGEN1STBY	1	R/W	RESETB	0x0	VGEN1 controlled by standby
VUSBSEL	2	R/W	NONE	*	Slave or Host configuration for VBUS
VUSBEN	3	R/W	RESETB	0x1	VUSB enable (PUMS4:1=[0100]). Also reset to 1 by invalid VBUS
VDACEN	4	R/W	NONE	*	VDAC enable
VDACSTBY	5	R/W	RESETB	0x0	VDAC controlled by standby
VDACMODE	6	R/W	RESETB	0x0	VDAC operating mode
Unused	9-7	R		0x0	Not available
VREFDDREN	10	R/W	NONE	*	VREFDDR enable
VGEN2CONFIG	11	R/W	NONE	*	PUMS5 Tied to ground = 0: VGEN2 with external PNP PUMS5 Tied to VCROREDIG =1:VGEN2 internal PMOS
VGEN2EN	12	R/W	NONE	*	VGEN2 enable
VGEN2STBY	13	R/W	RESETB	0x0	VGEN2 controlled by standby
VGEN2MODE	14	R/W	RESETB	0x0	VGEN2 operating mode
VPLLEN	15	R/W	NONE	*	VPLL enable
VPLLSTBY	16	R/W	RESETB	0x0	VPLL controlled by standby
VUSB2CONFIG	17	R/W	NONE	*	PUMS5 Tied to ground = 0: VUSB2 with external PNP PUMS5 Tied to VCROREDIG =1:VUSB2 internal PMOS
VUSB2EN	18	R/W	NONE	*	VUSB2 enable

Table 137. Register 32, Regulator Mode 0

Name	Bit #	R/W	Reset	Default	Description
VUSB2STBY	19	R/W	RESETB	0x0	VUSB2 controlled by standby
VUSB2MODE	20	R/W	RESETB	0x0	VUSB2 operating mode
Unused	23-21	R		0x0	Not available

Table 138. Register 33, GPIOLV0 Control

Name	Bit #	R/W	Reset	Default	Description
DIR	0	R/W	RESETB	0x0	GPIOLV0 direction 0: Input 1: Output
DIN	1	R/W	RESETB	0x0	Input state of GPIOLV0 pin 0: Input low 1: Input High
DOUT	2	R/W	RESETB	0x0	Output state of GPIOLV0 pin 0: Output Low 1: Output High
HYS	3	R/W	RESETB	0x1	Hysteresis 0: CMOS in 1: Hysteresis
DBNC[1:0]	5-4	R/W	RESETB	0x0	GPIOLV0 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce
INT[1:0]	7-6	R/W	RESETB	0x0	GPIOLV0 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges
PKE	8	R/W	RESETB	0x0	Pad keep enable 0: Off 1: On
ODE	9	R/W	RESETB	0x0	Open drain enable 0: CMOS 1: OD
DSE	10	R/W	RESETB	0x0	Drive strength enable 0: 4.0 mA 1: 8.0 mA
PUE	11	R/W	RESETB	0x1	Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default)
PUS[1:0]	13-12	R/W	RESETB	0x3	Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up

Table 138. Register 33, GPIOLV0 Control

Name	Bit #	R/W	Reset	Default	Description
SRE[1:0]	15-14	R/W	RESETB	0x0	Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast
Unused	23-16	R		0x00	Not available

Table 139. Register 34, GPIOLV1 Control

Name	Bit #	R/W	Reset	Default	Description
DIR	0	R/W	RESETB	0x0	GPIOLV1directon 0: Input 1: Output
DIN	1	R/W	RESETB	0x0	Input state of GPIOLV1 pin 0: Input low 1: Input High
DOUT	2	R/W	RESETB	0x0	Output state of GPIOLV1 pin 0: Output Low 1: Output High
HYS	3	R/W	RESETB	0x1	Hysteresis 0: CMOS in 1: Hysteresis
DBNC[1:0]	5-4	R/W	RESETB	0x0	GPIOLV1 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce
INT[1:0]	7-6	R/W	RESETB	0x0	GPIOLV1 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges
PKE	8	R/W	RESETB	0x0	Pad keep enable 0: Off 1: On
ODE	9	R/W	RESETB	0x0	Open drain enable 0: CMOS 1: OD
DSE	10	R/W	RESETB	0x0	Drive strength enable 0: 4.0 mA 1: 8.0 mA
PUE	11	R/W	RESETB	0x1	Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default)
PUS[1:0]	13:12	R/W	RESETB	0x3	Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up

Table 139. Register 34, GPIOLV1 Control

Name	Bit #	R/W	Reset	Default	Description
SRE[1:0]	15-14	R/W	RESETB	0x0	Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast
Unused	23-16	R		0x00	Not available

Table 140. Register 35, GPIOLV2 Control

Name	Bit #	R/W	Reset	Default	Description
DIR	0	R/W	RESETB	0x0	GPIOLV2 direction 0: Input 1: Output
DIN	1	R/W	RESETB	0x0	Input state of GPIOLV2 pin 0: Input low 1: Input High
DOUT	2	R/W	RESETB	0x0	Output state of GPIOLV2 pin 0: Output Low 1: Output High
HYS	3	R/W	RESETB	0x1	Hysteresis 0: CMOS in 1: Hysteresis
DBNC[1:0]	5-4	R/W	RESETB	0x0	GPIOLV2 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce
INT[1:0]	7-6	R/W	RESETB	0x0	GPIOLV2 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges
PKE	8	R/W	RESETB	0x0	Pad keep enable 0: Off 1: On
ODE	9	R/W	RESETB	0x0	Open drain enable 0: CMOS 1: OD
DSE	10	R/W	RESETB	0x0	Drive strength enable 0: 4.0 mA 1: 8.0 mA
PUE	11	R/W	RESETB	0x1	Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default)
PUS[1:0]	13-12	R/W	RESETB	0x3	Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up

Table 140. Register 35, GPIOLV2 Control

Name	Bit #	R/W	Reset	Default	Description
SRE[1:0]	15-14	R/W	RESETB	0x0	Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast
Unused	23-16	R		0x00	Not available

Table 141. Register 36, GPIOLV3 Control

Name	Bit #	R/W	Reset	Default	Description
DIR	0	R/W	RESETB	0x0	GPIOLV3 direction 0: Input 1: Output
DIN	1	R/W	RESETB	0x0	Input state of GPIOLV3 pin 0: Input low 1: Input High
DOUT	2	R/W	RESETB	0x0	Output state of GPIOLV3 pin 0: Output Low 1: Output High
HYS	3	R/W	RESETB	0x1	Hysteresis 0: CMOS in 1: Hysteresis
DBNC[1:0]	5-4	R/W	RESETB	0x0	GPIOLV3 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce
INT[1:0]	7-6	R/W	RESETB	0x0	GPIOLV3 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges
PKE	8	R/W	RESETB	0x0	Pad keep enable 0: Off 1: On
ODE	9	R/W	RESETB	0x0	Open drain enable 0: CMOS 1: OD
DSE	10	R/W	RESETB	0x0	Drive strength enable 0: 4.0 mA 1: 8.0 mA
PUE	11	R/W	RESETB	0x1	Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default)
PUS[1:0]	13-12	R/W	RESETB	0x3	Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up

Table 141. Register 36, GPIOLV3 Control

Name	Bit #	R/W	Reset	Default	Description
SRE[1:0]	15-14	R/W	RESETB	0x0	Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast
Unused	23-16	R		0x00	Not available

Table 142. Register 37, USB timing

Name	Bit #	R/W	Reset	Default	Description
DEVICE_WAKE_UP[3:0]	3-0	R/W	MUSBRSTB	0x0	The periodical sampling time of the ID line in the Power-Save mode and Standby mode; the periodical time of ADC conversion of the resistance at ID pin when RAW DATA = 0. 0000: 50 ms 0001: 100 ms 0010: 150 ms 0011: 200 ms 0100: 300 ms
KEYPRESS[3:0]	7-4	R/W	MUSBRSTB	0x0	Normal key press duration 0000: 100 ms 0001: 200 ms 0010: 300 ms ...
LONG_KEYPRESS[3:0]	11-8	R/W	MUSBRSTB	0x0	Long key press duration 0000: 300 ms 0001: 400 ms 0010: 500 ms ...
SWITCHING_WAIT	15-12	R/W	MUSBRSTB	0x0	Waiting time before switching the analog or digital switches: 0000: 10 ms 0001: 30 ms 0010: 50 ms ...
TD	19-16	R/W	MUSBRSTB	0x0	Time delay to start the powered accessory identification flow after detecting the bus voltage 0000: 100 ms 0001: 200 ms 0010: 300 ms 0011: 400 ms 0100: 500 ms ... 1111:1600 ms The time for no activity in the switches before entering the Power Save mode automatically for Audio Type 1 or TTY device 0000: 1 s 0001: 2 s ... 1001:10s ... 1111:16 s

Table 142. Register 37, USB timing

Name	Bit #	R/W	Reset	Default	Description
Unused	22-20	R		0x0	Not available
READVALID	23	R	MUSBRSTB	0x0	Read data valid 0: Data not valid 1: Data valid

Table 143. Register 38, USB Button

Name	Bit #	R/W	Reset	Default	Description
Send_End	0	R/C	MUSBRSTB	0x0	1: the Send_End button is pressed
S1	1	R/C	MUSBRSTB	0x0	1: button 1 is pressed
S2	2	R/C	MUSBRSTB	0x0	1: button 2 is pressed
S3	3	R/C	MUSBRSTB	0x0	1: button 3 is pressed
S4	4	R/C	MUSBRSTB	0x0	1: button 4 is pressed
S5	5	R/C	MUSBRSTB	0x0	1: button 5 is pressed
S6	6	R/C	MUSBRSTB	0x0	1: button 6 is pressed
S7	7	R/C	MUSBRSTB	0x0	1: button 7 is pressed
S8	8	R/C	MUSBRSTB	0x0	1: button 8 is pressed
S9	9	R/C	MUSBRSTB	0x0	1: button 9 is pressed
S10	10	R/C	MUSBRSTB	0x0	1: button 10 is pressed
S11	11	R/C	MUSBRSTB	0x0	1: button 11 is pressed
S12	12	R/C	MUSBRSTB	0x0	1: button 12 is pressed
ERROR	13	R/C	MUSBRSTB	0x0	1: button error occurred
UNKNOWN	14	R/C	MUSBRSTB	0x0	1: an unknown button is pressed
Unused	23-15	R		0x000	Not available

Table 144. Register 39, USB Control

Name	Bit #	R/W	Reset	Default	Description
Wait	0	R/W	MUSBRSTB	0x1	Wait or not to wait for the command from the baseband before turning on the analog or digital switches for attached accessory 0: Wait until this bit is changed to 1. Turn on the switches immediately when this bit is changed to 1. 1: Wait for only the time programmed by the Switching Wait bits in Timing Set 2 register before turning on the switches.
Manual S/W	1	R/W	MUSBRSTB	0x1	Manual or automatic switching of the switches 0: manual: the switches are controlled by the Manual S/W registers. 1: auto: the switches are controlled by the Device Type registers
RAWDATA	2	R/W	MUSBRSTB	0x1	Interrupt behavior selection 0: Enable the ADC conversion periodically and report the ADC Result changes on ID pin to the host. 1: Enable the key press monitor circuit to detect the ID pin status changes and report the key press events to the host.

Table 144. Register 39, USB Control

Name	Bit #	R/W	Reset	Default	Description
SWITCH_OPEN	3	R/W	MUSBRSTB	0x1	Switch connection selection 0: Open all switches 1: Switch selection according to the Manual S/W bit.
RESET	4	RWM	MUSBRSTB	0x0	Soft reset. When written to 1, the IC is reset. Once the reset is complete, the RST bit is set and the RESET bit is cleared automatically. 1: to soft-reset the IC
TTY_SPKL	5	R/W	MUSBRSTB	0x0	SPK_L to DM switch control 0: Turn off the SPK_L to DM switch 1: Turn on the SPK_L to DM switch for TTY
RST	6	R/C	MUSBRSTB	X	This bit indicates if a chip reset has occurred. This bit will be cleared once being read. 0: no. 1: Yes.
ACTIVE	7	R/W	MUSBRSTB	X	Indicate either the device is in Active mode 0: Standby 1: Active
CLK_RST	8	R/C	MUSBRST	0x1	Not available
VOTGEN	9	R/W	RESETB	0x0	Enables the OTG switch and the GOTG switch
Unused	10	R		0x0	Not available
Reserved	11	R	NONE	0x0	Reserved
SWHOLD	12	R/W	MUSBRSTB	0x1	Switch Hold 0: Run state machine and allow detection of accessory 1: Holds off state machine until baseband comes up
Reserved	14-13	R	NONE	0x0	Reserved
VBUS SWITCHING[1:0]	16-15	R/W	MUSBRSTB	0x0	VBUS line switching configuration when Manual S/W = 0 00: open all switches MOTG, M0 01: N/A 10: VBUS connects to MIC. M0, MOTG. Others: open all switches connected to the VBUS line
DP SWITCHING[2:0]	19-17	R/W	MUSBRSTB	0x0	DP line switching configuration when Manual S/W = 0 000: open all switches 001: DP connected to D+, DM connected to D- 010: DP connected to SPK_R, DM connected to SPK_L 011: DP connected to RxD, DM connected to TxD Others: open all switches connected to the DP pin and DM pin
DM SWITCHING[2:0]	22-20	R/W	MUSBRSTB	0x0	DM line switching configuration when Manual S/W = 0 000: open all switches 001: DP connected to D+, DM connected to D- 010: DP connected to SPK_R, DM connected to SPK_L 011: DP connected to RxD, DM connected to TxD Others: open all switches connected to the DP pin and DM pin
READVALID	23	R	MUSBRSTB	0x0	Read data valid 0: Data not valid 1: Data valid

Table 145. Register 40, USB Device Type

Name	Bit #	R/W	Reset	Default	Description
Audio Type 1	0	R	MUSBRSTB	0x0	1: An audio type 1 accessory is attached
Audio Type 2	1	R	MUSBRSTB	0x0	1: An audio type 2 accessory is attached
USB	2	R	MUSBRSTB	0x0	1: A USB host is attached
UART	3	R	MUSBRSTB	0x0	1: A UART cable is attached
5W CHG	4	R	MUSBRSTB	0x0	1: A 5-wire charger (type 1 or 2) is attached
USB CHG	5	R	MUSBRSTB	0x0	1: A USB charger is attached
DEDICATED CHG	6	R	MUSBRSTB	0x0	1: A dedicated charger is attached
USB OTG	7	R	MUSBRSTB	0x0	1: A USB OTG accessory is attached
PPD	8	R	MUSBRSTB	0x0	1: A phone powered device is attached
TTY	9	R	MUSBRSTB	0x0	1: A TTY converter is attached
A/V	10	R	MUSBRSTB	0x0	1: An audio/video cable is attached
AVCHRG	11	R	MUSBRSTB	0x0	1: An audio/video charger is attached
USBJIG1	12	R	MUSBRSTB	0x0	1: A USB jig cable 1 is attached
USBJIG2	13	R	MUSBRSTB	0x0	1: A USB jig cable 2is attached
UARTJIG1	14	R	MUSBRSTB	0x0	1: A UART jig cable 1is attached
UARTJIG2	15	R	MUSBRSTB	0x0	1: A UART jig cable 2 is attached
ID_FACTORY	16	R	MUSBRSTB	0x0	1: A factory cable is attached
UNK_DEVICE	17	R	MUSBRSTB	0x0	1: Device not recognized
Unused	18	R		0x0	Not available
ADCIDRESULT[4:0]	23-19	R	MUSBRSTB	0x00	ADC result value of the resistance at ID pin

Table 146. Register 41 and 42, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	0-23	R		0x000000	Not available

Table 147. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description
ADEN	0	R/W	DIGRESETB	0x0	Enables ADC from the low power mode
ADSTART	1	R/W	DIGRESETB	0x0	Request a start of the ADC Reading Sequencer
ADCONT	2	R/W	DIGRESETB	0x0	Run ADC reads continuously when high or one time when low. Note that the TSSTART request will have higher priority
ADHOLD	3	R/W	DIGRESETB	0x0	Hold the ADC reading Sequencer while saved ADC results are read from SPI
ADSTOP[2:0]	6-4	R/W	DIGRESETB	0x0	Channel Selection to stop when complete. Always start at 000 and read up to and including this channel value.
Spare	7	R/W	DIGRESETB	0x0	Not available
THERM	8	R/W	DIGRESETB	0x0	0 = Disable manual LED control. 1= Enable manual LED control
Spare	11-9	R/W	DIGRESETB	0x0	Not available

Table 147. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description
TSEN	12	R/W	DIGRESETB	0x0	Enable the Touch screen from low power mode.
TSSTART	13	R/W	DIGRESETB	0x0	Request a start of the ADC Reading Sequencer for Touch screen readings.
TSCONT	14	R/W	DIGRESETB	0x0	Run ADC reads of Touch screen continuously when high or one time when low.
TSHOLD	15	R/W	DIGRESETB	0x0	Hold the ADC reading Sequencer while saved Touch screen results are read from SPI
TSSTOP[2:0]	18-16	R/W	DIGRESETB	0x0	Just like the ADSTOP above, but for the Touchscreen read programming. This will allow independent code for ADC Sequence readings and touchscreen ADC Sequence readings.
Spare	19	R/W	DIGRESETB	0x0	Not available
TSPENDETEN	20	R/W	DIGRESETB	0x0	Enable the Touchscreen Pen Detection. Note that TSEN must be off for Pen Detection.
Spare	23-21	R/W	DIGRESETB	0x0	Not available

Table 148. Register 44, ADC 1

Name	Bit #	R/W	Reset	Default	Description
ADDLY1[3:0]	3-0	R/W	DIGRESETB	0x0	This will allow delay before the ADC readings.
ADDLY2[3:0]	7:4	R/W	DIGRESETB	0x0	This will allow delay between each of ADC readings in a set.
ADDLY3[3:0]	11-8	R/W	DIGRESETB	0x0	This will allow delay after the set of ADC readings. This delay is only valid between subsequent wrap around reading sequences with ADCONT
TSDLY1[3:0]	15-12	R/W	DIGRESETB	0x0	This will allow delay before the ADC Touch screen readings. This is like the ADDLY1, but allows independent programming of touchscreen readings from general purpose ADC readings to prevent code replacement in the system.
TSDLY2[3:0]	19-16	R/W	DIGRESETB	0x0	This will allow delay between each of ADC Touch screen readings in a set. This is like the ADDLY2, but allows independent programming of touchscreen readings from general purpose ADC readings to prevent code replacement in the system.
TSDLY3[3:0]	23-20	R/W	DIGRESETB	0x0	This will allow delay after the set of ADC Touch screen readings. This delay is only valid between subsequent wrap around reading sequences with TSCONT mode. This is like the ADDLY3, but allows independent programming of touchscreen readings from general purpose ADC readings to prevent code replacement in the system.

Table 149. Register 45, ADC 2

Name	Bit #	R/W	Reset	Default	Description
ADSEL0[3:0]	3-0	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT0
ADSEL1[3:0]	7-4	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT1
ADSEL2[3:0]	11-8	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT2
ADSEL3[3:0]	15-12	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT3

Table 149. Register 45, ADC 2

Name	Bit #	R/W	Reset	Default	Description
ADSEL4[3:0]	19-16	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT4
ADSEL5[3:0]	23-20	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT5

Table 150. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description
ADSEL6[3:0]	3-0	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT6
ADSEL7[3:0]	7-4	R/W	DIGRESETB	0x0	Channel Selection to place in ADRESULT7
TSSEL0[1:0]	9-8	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT0. Select the action for the Touchscreen; 00 = dummy to discharge TSREF capacitance, 01 = to read X-plate, 10 = to read Y-plate, and 11 = to read Contact.
TSSEL1[1:0]	11-10	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT1. See TSSEL0 for modes.
TSSEL2[1:0]	13-12	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT2. See TSSEL0 for modes.
TSSEL3[1:0]	15-14	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT3. See TSSEL0 for modes.
TSSEL4[1:0]	17-16	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT4. See TSSEL0 for modes.
TSSEL5[1:0]	19-18	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT5. See TSSEL0 for modes.
TSSEL6[1:0]	21-20	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT6. See TSSEL0 for modes.
TSSEL7[1:0]	23-22	R/W	DIGRESETB	0x0	Touchscreen Selection to place in ADRESULT7. See TSSEL0 for modes.

Table 151. Register 47, ADC 4

Name	Bit #	R/W	Reset	Default	Description
Unused	1-0	R		0x0	Not available
ADRESULT0[9:0]	11-2	R	DIGRESETB	0x000	ADC Result for ADSEL0
Unused	13-12	R		0x0	Not available
ADRESULT1[9:0]	23-14	R	DIGRESETB	0x000	ADC Result for ADSEL1

Table 152. Register 48, ADC5

Name	Bit #	R/W	Reset	Default	Description
Unused	1-0	R		0x0	Not available
ADRESULT2[9:0]	11-2	R	DIGRESETB	0x000	ADC Result for ADSEL2
Unused	13-12	R		0x0	Not available
ADRESULT3[9:0]	23-14	R	DIGRESETB	0x000	ADC Result for ADSEL3

Table 153. Register 49, ADC6

Name	Bit #	R/W	Reset	Default	Description
Unused	1-0	R		0x0	Not available
ADRESULT4[9:0]	11-2	R	DIGRESETB	0x000	ADC Result for ADSEL4
Unused	13-12	R		0x0	Not available
ADRESULT5[9:0}	23-14	R	DIGRESETB	0x000	ADC Result for ADSEL5

Table 154. Register 50, ADC7

Name	Bit #	R/W	Reset	Default	Description
Unused	1:0	R		0x0	Not available
ADRESULT6[9:0]	11-2	R	DIGRESETB	0x000	ADC Result for ADSEL6
Unused	13-12	R		0x0	Not available
ADRESULT7[9:0]	23-14	R	DIGRESETB	0x000	ADC Result for ADSEL7

Table 155. Register 51, Input Monitoring

Name	Bit #	R/W	Reset	Default	Description
VBAT_TRKL[1:0]	1-0	R/W	RTCPORB	0x0	Trickle1 to Trickle2 change over threshold 00: 2.8 V 01: 2.9 V 10: 3.0 V 11: 3.1 V
Reserved	2	R	NONE	0x0	Reserved
CHREN	3	R/W	RTCPORB	0x1	Charger enable
LOWBATT[1:0]	5-4	R/W	RTCPORB	0x3	Turn on detection threshold and low battery warning threshold
Reserved	23-6	R/W	NONE	0x00000	Reserved

Table 156. Register 52, Input Debounce

Name	Bit #	R/W	Reset	Default	Description
Reserved	1-0	R/W	NONE	0x0	Reserved
VBATTDB[1:0]	3-2	R/W	RESETB	0x3	Battery voltage debounce
VBUSDB[1:0]	5-4	R/W	RESETB	0x03	VBUS debounce
Reserved	9-6	R/W	NONE	0x0	Reserved
CHRGLEDOVRD	10	R/W	RESETB	0x0	LED override
Reserved	13-11	R/W	NONE	0x0	Reserved
SUP_OVP_DB[1:0]	15-14	R/W	RESETB	0x3	VBUS over voltage debounce
DIE_TEMP_DB[1:0]	17-16	R/W	RESETB	0x3	Die Temp Comparator Debounce
Reserved	23-18	R	NONE	0x00	Reserved

Table 157. Register 53, VBUS Monitoring

Name	Bit #	R/W	Reset	Default	Description
VBUSTL[2:0]	2-0	R/W	RESETB	0x3	VBUS threshold low
VBUSTH[2:0]	5-3	R/W	RESETB	0x3	VBUS threshold high
Reserved	23-6	R/W	NONE	0x00000	Reserved

Table 158. Register 54, LED Control

Name	Bit #	R/W	Reset	Default	Description
CHRGLEDRPER[1:0]	1-0	R/W	RESETB	0x0	LED red repetition period
CHRGLEDRRAMP	2	R/W	RESETB	0x0	LED red channel driver ramp enable
CHRGLEDRDC[5:0]	8-3	R/W	RESETB	0x00	LED red channel driver duty cycle
CHRGLEDR[1:0]	10-9	R/W	RESETB	0x3	LED red driver current setting
CHRGLEDREN	11	R/W	RESETB	0x0	LED red enable
CHRGLEDGPER[1:0]	13-12	R/W	RESETB	0x0	LED green repetition period
CHRGLEDGRAMP	14	R/W	RESETB	0x0	LED green channel driver ramp enable
CHRGLEDGDC[5:0]	20-15	R/W	RESETB	0x00	LED green channel driver duty cycle
CHRGLEDG[1:0]	22-21	R/W	RESETB	0x3	LED green driver current setting
CHRGLEDGEN	23	R/W	RESETB	0x0	LED green enable

Table 159. Register 55, PWM Control

Name	Bit #	R/W	Reset	Default	Description
PWM1DUTY[5:0]	5-0	R/W	RESETB	0x00	PWM1 Duty Cycle
PWMCLKDIV[5:0]	11-6	R/W	RESETB	0x00	PWM1 Clock Divide Setting
PWM2DUTY[5-0]	17-12	R/W	RESETB	0x00	PWM2 Duty Cycle
PWM2CLKDIV[5:0]	23-18	R/W	RESETB	0x00	PWM2 Clock Divide Setting

Table 160. Register 56 to 63, Unused

Name	Bit #	R/W	Reset	Default	Description
Unused	0-23	R		0x000000	Not available

8 Typical Applications

Figure 38 presents a typical application diagram of the MC34708 PMIC together with its functional components. For details on component references and additional components such as filters, refer to the individual sections.

8.1 Application Diagram

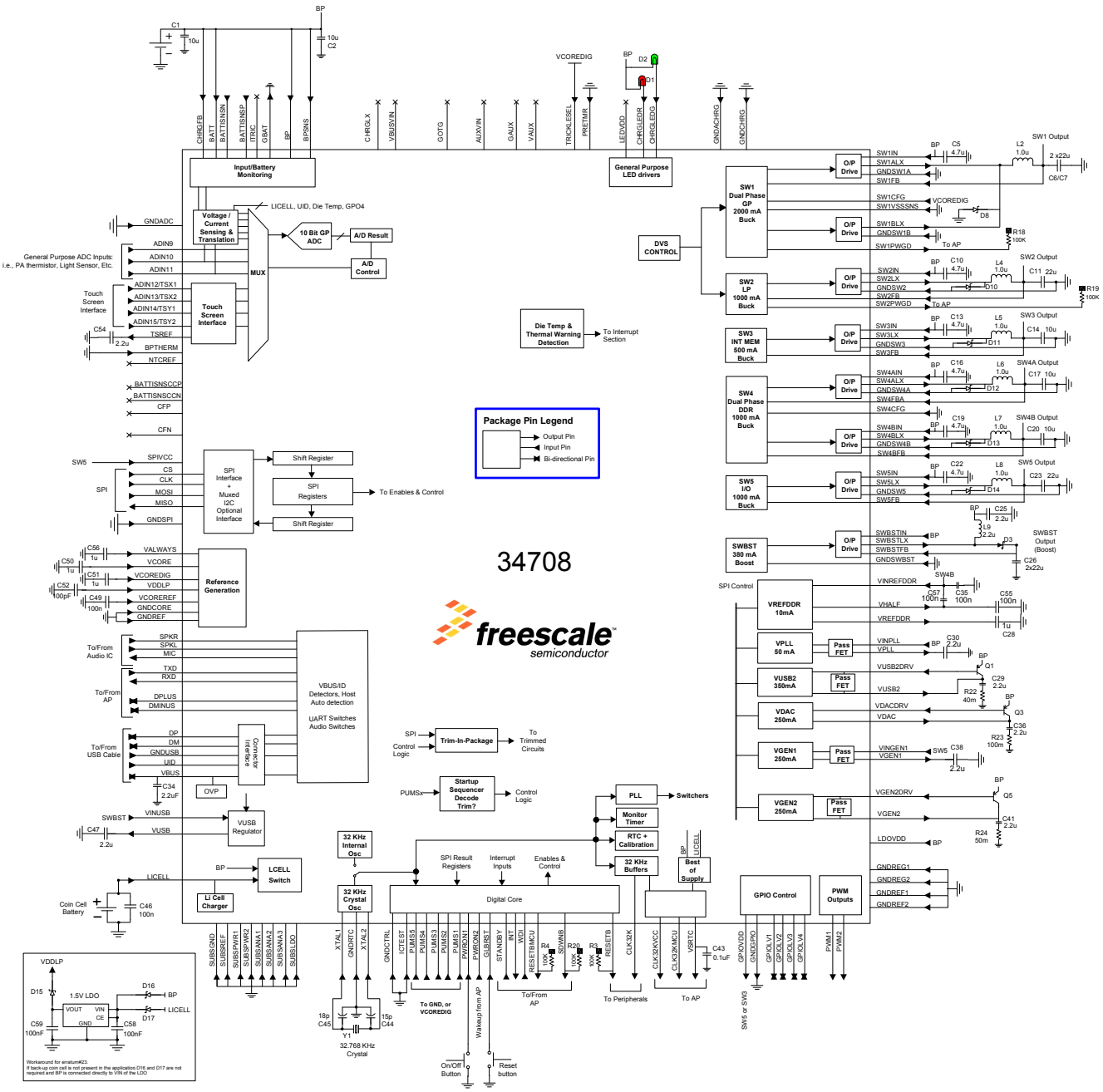


Figure 38. Typical Application Schematic

8.2 Bill of Material

The following table provides a complete list of the recommended components on a full featured system using the MC34708 Device. Critical components such as inductors, transistors, and diodes are provided with a recommended part number, but equivalent components may be used.

Table 161. MC34708 Bill of Material (84)

Item	Quantity	Component	Description	Vendor	Comments
1	1		MC34708	Freescale	PMIC
Battery Interface					
2	1	C1	10 μF	TDK	Battery Filter
3	2	R1	20 mOhm		Battery Sense (Optional for battery current sensing)
4	1	C2	10 μF		BP/ buck charging capacitor
5	1	C67	1 uF		VBUS 1 uF input cap
6	1	D2	Green LED		Green general purpose LED indicator
7	1	D1	Red LED		Red General purpose LED indicator
Miscellaneous					
8	1	C56	1.0 μF		VALWAYS
9	1	C43	100 nF		VSRTC
10	1	C50	1.0 μF		VCORE
11	1	C51	1.0 μF		VCOREDIG
12	1	C52	100 pF		VDDLP
13	1	C49	100 nF		VCOREREF
14	1	C46	100 nF		Coin cell
15	1	Y1	Crystal 32.768 kHz CC7		Oscillator
16	1	C44	18 pF		Oscillator load capacitor
17	1	C45	18 pF		Oscillator load capacitor
18	2	R3, R4	100 k		RESETB, RESETBMCU Pull-ups
19	1	R20	100 k		SDWNB Pull-up
Boost					
20	1	L9	2.2 μH LPS3015-222ML	Coilcraft	Boost Inductor
21	1	D3	Diode BAS52	Infineon	Boost diode
22	1	C26	2.2 μF 16 V		Boost Output Capacitor
23	2	C25	22 μF		Boost Input Capacitor

Table 161. MC34708 Bill of Material [84]

Item	Quantity	Component	Description	Vendor	Comments
SW1					
24	2	L2, L3	1.0 μH VLS201612ET-1R0N	TDK	Buck 1 Inductor (I_{MAX} < 1.6 Amps)
			1.0 μH VLS252010ET-1R0N	TDK	Optional dual phase Inductor ($I_{MAX} \leq$ 2.0 Amps)
			1.0 μH BRL3225T1ROM	Taiyo Yuden	Optional single Phase inductor (I_{MAX} < 1.6 Amps)
			1.0 uH LPS4012-102NL	Coilcraft	Optional single phase inductor ($I_{MAX} \leq$ 2.0 Amps)
25	2	C6, C7	22 μF		Buck 1 Output Capacitor
26	1	C5	4.7 μF		Buck 1 Input Capacitor
27	1	D8	Diode BAS3010-03LRH	Infineon	SW1LX diode
SW2					
28	1	L4	1.0 μH VLS252010ET-1R0N	TDK	Buck 2 Inductor
29	1	C11	22 μF		Buck 2 Output Capacitor
30	1	C10	4.7 μF		Buck 2 Input Capacitor
31	1	D10	Diode BAS3010-03LRH	Infineon	SW2LX diode
SW3					
32	1	L5	1.0 μH VLS201612ET-1R0N	TDK	Buck 3 Inductor
33	1	C14	10 μF		Buck 3 Output Capacitor
34	1	C13	4.7 μF		Buck 3 Input Capacitor
35	1	D11	Diode BAS3010-03LRH	Infineon	SW3LX diode
SW4A					
36	1	L6	1.0 μH VLS201612ET-1R0N	TDK	Buck 4A Inductor
37	0		1.0 μH VLS252010ET-1R0N	TDK	Optional Inductor
38	1	C17	10 μF		Buck 4A Output Capacitor
39	1	C16	4.7 μF		Buck 4A Input Capacitor
40	1	D12	Diode BAS3010-03LRH	Infineon	SW4ALX diode
SW4B					
41	1	L7	1.0 μH VLS201612ET-1R0N	TDK	Buck 4B Inductor
42	0	-	1.0 μH VLS25010ET-1R0N	TDK	Optional Inductor
43	1	C20	10 μF		Buck 4B Output Capacitor
44	1	C19	4.0 μF		Buck 4B Input Capacitor
45	1	D13	Diode BAS3010-03LRH	Infineon	SW4BLX diode
SW5					
46	1	L8	1.0 μH VLS252010ET-1R0N	TDK	Buck 5 Inductor
47	1	C23	22 μF		Buck 5 Output Capacitor
48	1	C22	4.7 μF		Buck 5 Input Capacitor

Table 161. MC34708 Bill of Material [84]

Item	Quantity	Component	Description	Vendor	Comments
49	1	D14	Diode BAS3010-03LRH	Infineon	SW5LX diode
VPLL					
50	1	C30	2.2 μF		VPLL
VREFDDR					
51	1	C35	100 nF		VREFDDR input capacitor
52	1	C57	100 nF		VHALF 0.1 uF caps
53	1	C28	1.0 μF		VREFDDR
VDAC					
54	1	Q3	PNP Transistor • NSS12100UW3 • 2SB1733	On Semi Rohm	VDAC PNP
55	1	C36	2.2 μF		VDAC
56	1	R23	100 mΩ		Connect this resistor in series with the output capacitor to provide an extra series resistance of 100 mΩ for LDO stability.
VUSB2					
57	1	Q1	PNP transistor • NSS12100UW3 • 2SB1733	On Semi Rohm	VUSB2 PNP
58	1	C29	2.2 μF		VUSB2
59	1	R22	40 mΩ		Connect this resistor in series with the output capacitor to provide an extra series resistance of 40 mΩ for LDO stability.
VUSB					
60	1	C47	2.2 μF		VUSB
VGEN1					
61	1	C38	4.7 μF		VGEN1
VGEN2					
62	1	Q5	PNP Transistor • NSS12100UW3 • 2SB1733	On Semi Rohm	VGEN2 PNP
63	1	C41	2.2 μF		VGEN2
64	1	R24	50 mΩ		Connect this resistor in series with the output capacitor to provide an extra series resistance of 50 mΩ for LDO stability.
WORKAROUNDS					
65	1	U2	1.5 V LDO • NCP4682 • NCP4685	On Semi	1.5 V LDO for workaround. See erratum #23 on ER34708

Table 161. MC34708 Bill of Material [84]

Item	Quantity	Component	Description	Vendor	Comments
66	1	D15	Schottky diode		Low voltage Schottky diode
67	1	C58	100 nF		LDO input capacitor
68	1	C59	100 nF		LDO output capacitor

Notes

84. Freescale does not assume liability, endorse, or warrant components from external manufacturers referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

8.3 MC34708 Layout Guidelines

8.3.1 General board recommendations

1. It is recommended to use an 8 layer board stack-up arranged as follows:
- High current signal
- GND
- Signal
- Power
- Power
- Signal
- GND
- High current signal

2. Allocate TOP and BOTTOM PCB Layers for POWER ROUTING (high current signals), copper-pour the unused area.
3. Use internal layers sandwiched between two GND planes for the SIGNAL routing.

8.3.2 Component Placement

Sense resistors should be placed as Close to the IC as possible. Route the high current path flowing from VBATT to BATTISNSN as thick and as short as possible to reduce power losses.

8.3.3 General Routing Requirements

1. Some recommended things to keep in mind for manufacturability:
   - Via in pads require a 4.5 mil Minimum annular ring. Pad must be 9.0 mils larger than the hole
   - Max copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
   - Minimum allowed spacing between line and hole pad is 3.5 mils
   - Minimum allowed spacing between line and line is 3.0 mils
2. Care must be taken with SWxFB pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the SWxIN, SWx, SWxLX, SWBSTIN, SWBST, and SWBSTLX pins.
3. Shield feedback traces of the switching regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
4. Sense pins must be directly connected to the 0.02 Ohm sense resistor R1 (BATTISNSN and BATTISNSP).
5. Avoid coupling trace between important signal/low noise supplies (like VCOREREF, VCORE, VCOREDIG) from any switching node (i.e. SW1ALXx, SW2LXx, SW3LXx, SW4ALX, SW4BLX, SW5LXx and SWBSTLXx).
6. Make sure all components related to an specific block are referenced to the corresponding ground, e.g. all components related to the SW1 converter must referenced to GNDSW1A1 and GNDSW1A2.

8.3.4 Parallel Routing Requirements

1. SPI/I^2C signal routing:
- CLK is the fastest signal of the system, so it must be given special care. Here are some tips for routing the communication signals:
- To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

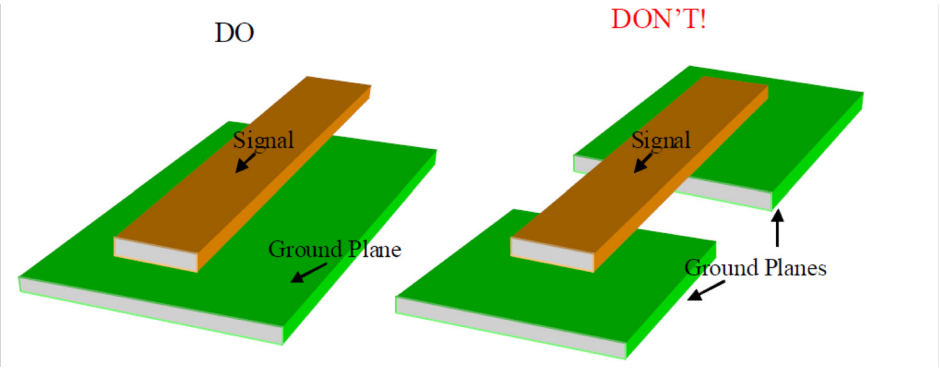


Figure 39. Recommended Shielding for Critical Signals.

- These signals can be placed on an outer layer of the board to reduce their capacitance in respect to the ground plane.
- The crystal connected to the XTAL1 and XTAL2 pins must not have a ground plane directly below.
- The following are clock signals: CLK, CLK32K, CLK32KMCU, XTAL1, and XTAL2. These signals must not run parallel to each other, or in the same routing layer. If it is necessary to run clock signals parallel to each other, or parallel to any other signal, then follow a MAX PARALLEL rule as follows:
    - Up to 1 inch parallel length – 25 mil minimum separation
    - Up to 2 inch parallel length – 50 mil minimum separation
    - Up to 3 inch parallel length – 100 mil minimum separation
    - Up to 4 inch parallel length – 250 mil minimum separation
    - Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

2. The R1 resistor must run in parallel to the BATTISNSN and BATTISNSP traces.

8.3.5 Differential Routing

1. DP and DM traces should be routed as 90 ohm differential signals.
2. DPLUS and DMINUS traces should be routed as 90 ohm differential signals.

8.3.6 Switching Regulator Layout Recommendations

1. Per design, the MC34708 is designed to operate with only 1 input bulk capacitor. However, it is recommended to add a high frequency filter input capacitor (CIN_hf), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
2. Make high-current ripple traces low inductance (short, high W/L ratio).
3. Make high-current traces wide or copper islands.
4. Make high-current traces SYMETRICAL for dual–phase regulators (SW1, SW4).

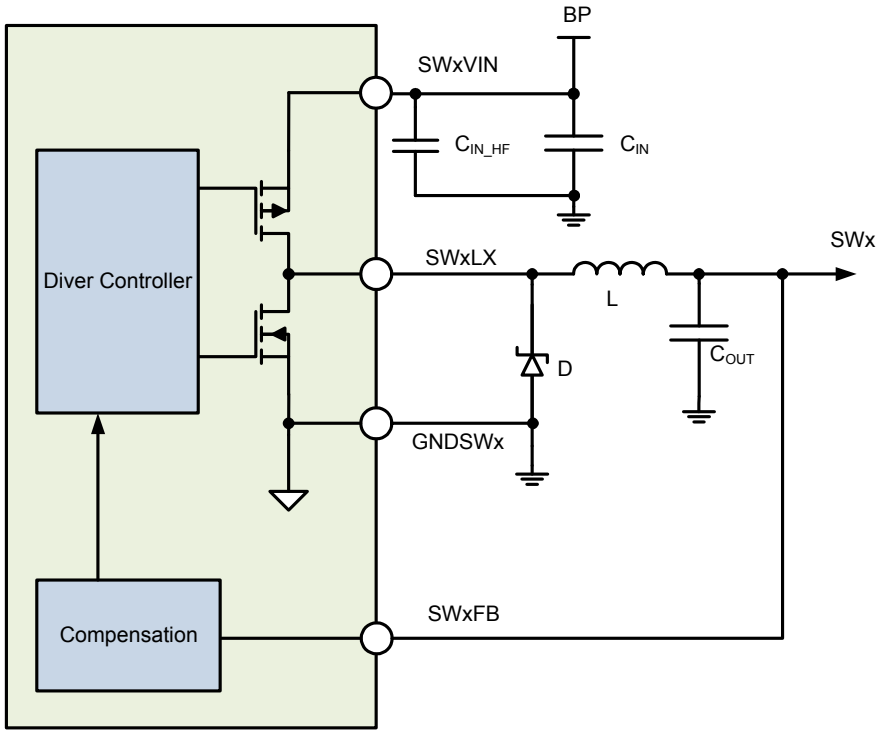


Figure 40. Generic Buck Regulator Architecture

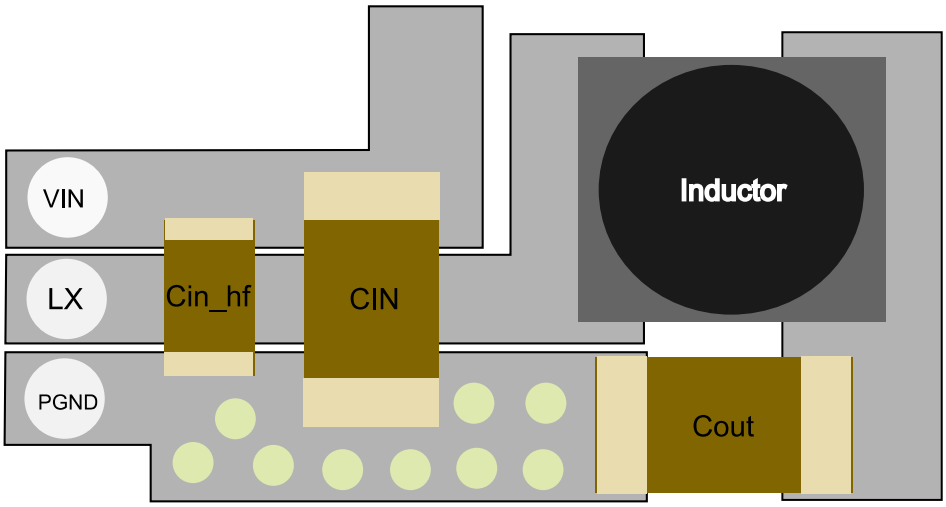


Figure 41. Recommended Layout for Switching Regulators.

8.4 Thermal Considerations

8.4.1 Rating Data

The thermal rating data of the packages has been simulated with the results listed in Table 5.

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. The generic name, Theta-JA, is expected to continue to be commonly used.

The JEDEC standards can be consulted at http://www.jedec.org/

8.4.2 Estimation of Junction Temperature

An estimation of the chip junction temperature TJ can be obtained from the equation

$T_J = T_A + (R_{\theta JA} \times P_D)$

with

T_A = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature TJ is estimated using the following equation

$T_J = T_B + (R_{\theta JB} \times P_D)$ with

T_B = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

See Thermal Characteristics for more details on thermal management.

9 Package Mechanical Dimensions

The MC34708 is offered in two pin compatible 206 pin MAPBGA packages, an 8.0x8.0 mm, 0.5 mm pitch package, and a 13x13 mm, 0.8 mm pitch package.

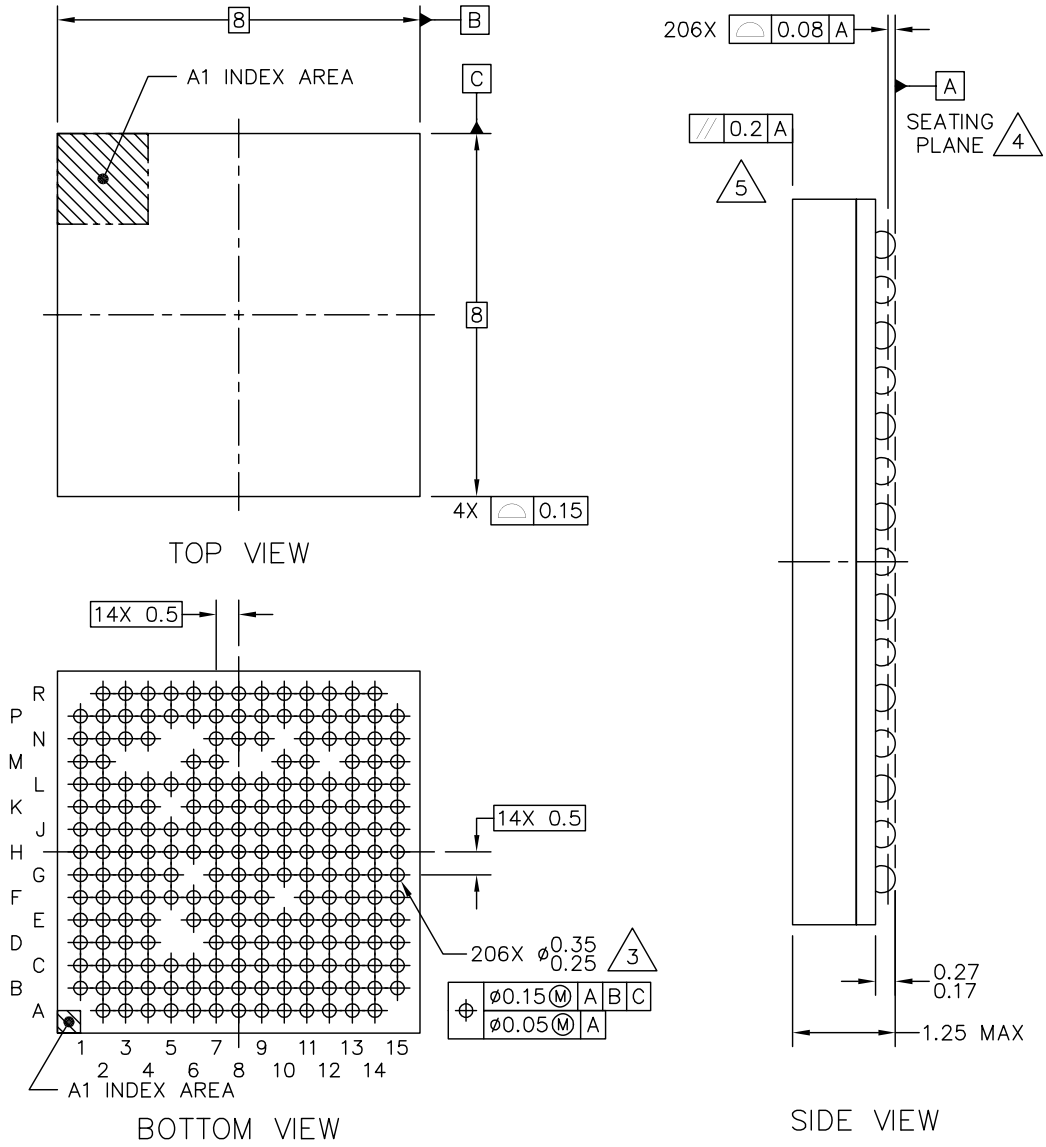
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 162. Package Drawing Information

Package	Suffix	Package Outline Drawing Number
206-pin MAPBGA (8 x 8), 0.5 mm	VK	98ASA00312D
206-pin MAPBGA (13 x 13), 0.8 mm	VM	98ASA00299D

Dimensions shown are provided for reference ONLY (For Layout and Design, refer to the Package Outline Drawing listed in the following figures).

9.1 206-pin MAPBGA (8 x 8), 0.5 mm



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TITLE: PBGA, THIN PROFILE, FINE PITCH, 206 I/O, 8 X 8 PKG, 0.5 MM PITCH (MAP)	DOCUMENT NO: 98ASA00312D	REV: O
	CASE NUMBER: 2187–01	16 DEC 2010
	STANDARD: JEDEC MO–275–CCCE–1	

VK SUFFIX (PB-FREE)
206-PIN
98ASA00312D
ISSUE 0

MC34708

NOTES:

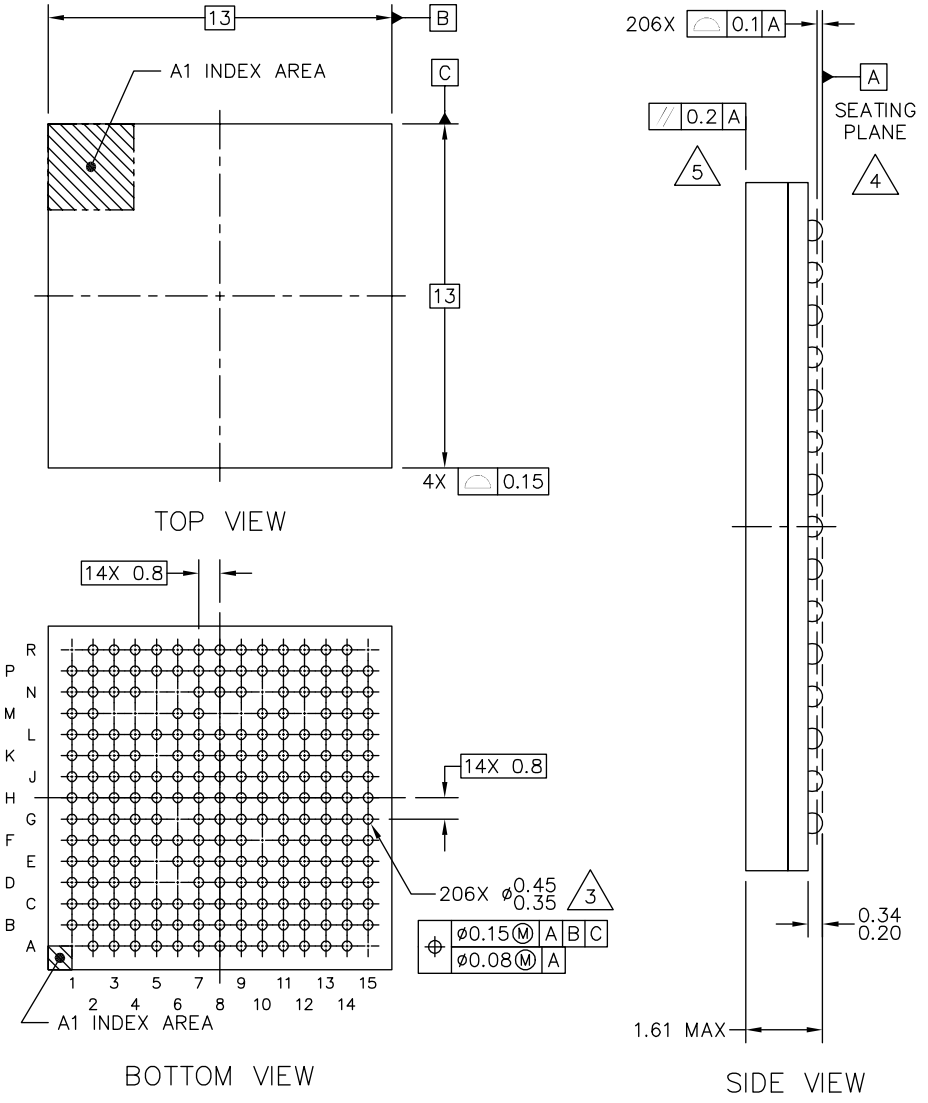
1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, THIN PROFILE, FINE PITCH, 206 I/O, 8 X 8 PKG, 0.5 MM PITCH (MAP)	DOCUMENT NO: 98ASA00312D	REV: O
	CASE NUMBER: 2187–01	16 DEC 2010
	STANDARD: JEDEC MO–275–CCCE–1	

VK SUFFIX (PB-FREE)
206-PIN
98ASA00312D
ISSUE 0

9.2 206-pin MAPBGA (13 x 13), 0.8 mm



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TITLE: PBGA, LOW PROFILE, FINE PITCH, 206 I/O, 13 X 13 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00299D	REV: A
	CASE NUMBER: 2178–01	18 FEB 2011
	STANDARD: JEDEC MO–275–HHAC–1	

VM SUFFIX (PB-FREE)
206-PIN
98ASA00299D
ISSUE A

MC34708

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, FINE PITCH, 206 I/O, 13 X 13 PKG, 0.8 MM PITCH (MAP)		DOCUMENT NO: 98ASA00299D	REV: A
		CASE NUMBER: 2178–01	18 FEB 2011
		STANDARD: JEDEC MO–275–HHAC–1	

VM SUFFIX (PB-FREE)
206-PIN
98ASA00299D
ISSUE A

10 Reference Section

Table 163. MC34708 Reference Documents

Reference	Description
MC34708ER	Errata

11 Revision History

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REVISION	DATE	DESCRIPTION OF CHANGES
6.0	7/2011	• Initial release
7.0	10/2011	• Corrected the two pins SW2PWGD and SDWNB, and associated drawings. • Changed LED Driver Electrical Specifications, VPLL Matching from 3.0 to 4.0% • Changed VPLL Electrical Specification, $t_{ON-VPLL}$ from 100 to 120 μs • Changed SWBST Electrical Specifications, I_{LEAK_SWBST} from 5.0 to 6.0 μA • Added Max limit to Charger Input Current Limit (Using the USB input). • Added note (61) to V_{REFDDR} • Changed $R_{USB\ ON}$ value to 5.0 typ, 8.0 max • Set MIC bias to 1.5 V, and changed ON resistance values to 75 typ and 150 max. • Added Efficiency values for all Buck Converter • Added diodes to the LX pin on SW1, SW2, SW3, SW4A, SW4B, and SW5. • Updated schematics to reflect the LX pin diodes on SW1, SW2, SW3, SW4A, SW4B, and SW5, and removed the 10 μF VBUSVIN input capacitor.

8.0	7/2012	• Removed charger and coulomb counter functionality throughout the document. Section 7.6 removed.
		• Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 38, Figure 20, Figure 26, Figure 28, Figure 30, Figure 31, Figure 40.
		• Update Table 3
		  • Pin function changed to “O” on pins VCORE, VCOREDIG, VALWAYS, VCOREREF, VDDLP, and TSREF.
		  • Pin function to “I” on pins ADIN11, TSX1/ADIN12, TSX2/ADIN13, TSY1/ADIN14 and TSY2/ADIN15
		  • Description for unsupported charger and coulomb counter pins modified.
		  • Clarified ICTEST description
		• Update Table 4 with maximum pin rating for all blocks.
		• Added Table 7 “Die Temp Debounce Settings”
		• Updated thermal monitor operation in section 5.2.1
		• Removed PRETMR, ITRICKLE, VSRT and ADC specifications in Table 9.
		• Changed typ current spec for ON Standby (LPM) from 260 uA to 340uA, changed ON Standby Digital Core from 370uA to 480uA and removed all charger conditions in Table 10.
		• Updated section 6.1 feature list
		• Renamed all instances of APSKIP to APS.
		• Updated Table 15: VSRTC quiescent current to 1.7uA @1.2V setting and 2.7uA @ 1.3V setting.
		• GLBRSTTMR[1:0], value “00” changed to Invalid option in Table 24.
		• Removed interrupt, mask and sense bit related to charger and coulomb counter in Table 21.
		• Changed debounce time for THERMxxx interrupts.
		• Updated SW4A/B operation and removed 3.3V setting from SW4A/B in section 7.5.4.6
		• Removed AUX attach in section 7.5.3.4
		• Replaced “Under Voltage Detection” event in section 7.5.3.5 with “BP lower than VBAT_TRKL” event.
		• Changed UVDET threshold to 3.1V (rising)/ 2.65V (falling) in Table 27
		• Added PWMPS mode description on Table 31
		• Changed quiescent currents for all switching regulators ISWxQ in PWMPS and APS modes.
		• LDO Short Circuit Protection feature no longer supported.
		• Changed ADC channels 4 and 7 to “Reserved”
		• Added Figure 19. Added section 7.8.3.
		• Removed VBATTREMTH specification from Table 77
		• Removed charger support from section 7.8.4
		• Removed IVBUS quiescent current specification for dedicated charger condition in Table 97
		• Updated components to BOM in section 8.2
		• Updated SPI register map
		  • Replaced Figures 42-45 with Table 104 SPI/I2C Register Map
		  • Updated Table 101 and Table 104 to match removed functionality
		• Updated Table 105 through Table 158 to match removed functionality

REVISION	DATE	DESCRIPTION OF CHANGES
9.0	10/2012	• Corrected pins E14, E15, and F7 in Table 3 • Corrected Figure 3, Ball Map.

10	2/2013	• Update table 3. Pin definition
		  • Pin TRICKLESEL, Function = I, Description = Connect to VCOREDIG
		  • Pin PRETMR, Function = I, Description = Connect to Ground
		  • Pin BPTHERM, Function = I, Description = Connect to Ground
		• Update Table 4. Maximum rating
		  • Update IC core Reference maximum pin voltages.
		  • Update LDO regulator maximum pin voltage.
		• Table 5. Note added to restrict operation at maximum temperature ratings.
		• Table 10. Update Mode descriptions.
		• Removed PWMPS mode on all Buck Switching regulators.
		• Corrected SWBST operating mode PWM to APS
		• Typical short circuit protection defined to 20% above I_{LMAX}
		• Remove Noise specifications from all LDO regulators.
		• Removed Short-circuit protection threshold specification from VUSB2, VDAC and VGEN1 and VUSB.
		• Removed Spurs specification on VDAC and VGEN1
		• Changed PSRR specifications for all LDO regulators to typical value only.
		• Changed typical $VPLL_{PSRR}$ specifications
		  • V_{IN}=UVDET: from 40 to 70 dB
		  • $V_{IN}=V_{NOM}$+1.0 V, >UVDET: from 60 to 75 dB
		• Changed typical $VUSB2_{PSRR}$ specifications
		  • $V_{IN}=VIN_{MIN}$ + 100 mV: from 40 to 30 dB
		  • $V_{IN}=V_{NOM}$+1.0 V: from 60 to 30 dB
		• Changed typical $VDAC_{PSRR}$ specifications
		  • $V_{IN}=VIN_{MIN}$ + 100 mV: from 40 to 50 dB
		  • $V_{IN}=V_{NOM}$+1.0 V: from 60 to 50 dB
		• Changed typical $VGEN1_{PSRR}$ specifications
		  • $V_{IN}=VIN_{MIN}$ + 100 mV: from 60 to 50 dB
		  • $V_{IN}=V_{NOM}$+1.0 V: from - to 45 dB
		• Changed typical $VUSB_{PSRR}$ specifications
		  • $V_{IN}=VIN_{MIN}$ + 100 mV: from 40 to 65 dB
		• Specified total series resistance of VGEN2 output capacitance to 60mΩ ±20% including capacitor ESR.
		• Changed ADC drift over temperate from 1 to 10 LSB
		• Update Bill of materials
		• Corrected sensing point for ADC channel 2, from BP to BPSENSE pin.
		• Table 81. LED driver control option x00 changed the CHRGLEDx status to Off.
		• Changed section 7.8.4.15 title to Device Detect mode
		• Updated figure 38
		• Updated General Purpose LED Drivers Current Programming
		• Corrected Table 14 VCOREDIG spec
		• Modified Table 82 LED current programming

	4/2013	• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph. Changed to Technical Data.
11	11/2013	• Updated section Oscillator Specifications. • Added note (38) to VSRTC Electrical Specifications table.

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11/2013

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